Distributed Amplifiers

Ali Medi

Outline

- Introduction
- DA principles of operation
- DA with artificial T-lines
- DAs with improved gain stages
- Noise in DAs
- DAs with tapered T-lines
- Loss compensation in DAs
- Transformer-based DA

Introduction

- Distributed amplifier basic idea first introduced in 1936 [Percival 36] to overcome traditional GBW limit of vacuum tube amplifiers.
- The name distributed amplifier first introduced in [Ginzton 48].
- The key idea is to absorb parasitic capacitances of the transistors into T-lines to improve the amplifier bandwidth.

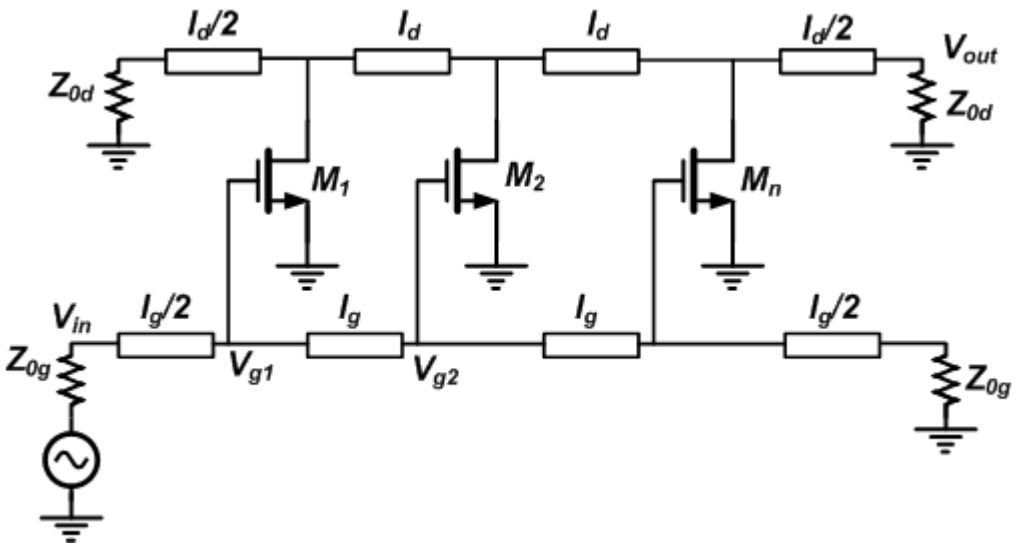
DA principles of operation

$$V_{g1} = V_{in} e^{-\theta_g/2}$$

$$V_{gk} = V_{in} e^{-(k-\frac{1}{2})\theta_g}$$

$$I_{dk} = g_{mk} V_{gk}$$

$$I_{out} = \frac{1}{2} \sum_{k=1}^{n} I_{dk} e^{-(n-k+\frac{1}{2})\theta_d}$$



$$\theta_{g,d} = \gamma_{g,d} l_{g,d} = (\alpha_{g,d} + j\beta_{g,d}) l_{g,d}$$

$$I_{out} = \frac{1}{2} V_{in} e^{-n\theta_d} e^{-(\theta_g-\theta_d)/2} \sum_{k=1}^{n} g_{mk} e^{-(k-1)(\theta_g-\theta_d)}$$

$$g_{mk} = g_m$$

$$I_{out} = \frac{1}{2} g_m V_{in} e^{-n\theta_d} e^{-(\theta_g-\theta_d)/2} \frac{1 - e^{-n(\theta_g-\theta_d)}}{1 - e^{-(\theta_g-\theta_d)}}$$

$$Z_{0g} = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}}$$

$$Z_{0d} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}}$$

DA principles of operation

$$A_v = \frac{1}{2} g_m Z_{0d} \frac{e^{-n\theta_d} - e^{-n\theta_g}}{e^{(\theta_g - \theta_d)/2} - e^{-(\theta_g - \theta_d)/2}}$$

For Loss-less T-lines ($\alpha_g = \alpha_d = 0$)

$$|A_v| = \frac{1}{2} g_m Z_{0d} \left| \frac{\sin \frac{n}{2}(\beta_g l_g - \beta_d l_d)}{\sin \frac{1}{2}(\beta_g l_g - \beta_d l_d)} \right|$$

Available power gain

$$G_p = \frac{\frac{1}{2} Z_{0d} |I_{out}|^2}{V_{in}^2 / 2Z_{0g}} = \frac{1}{4} g_m^2 Z_{0g} Z_{0d} \left| \frac{\sin \frac{n}{2}(\beta_g l_g - \beta_d l_d)}{\sin \frac{1}{2}(\beta_g l_g - \beta_d l_d)} \right|^2$$

For $\beta_g l_g = \beta_d l_d$

$$|A_v| = \frac{1}{2} n g_m Z_{0d}$$

$$G_p = \frac{1}{4} n^2 g_m^2 Z_{0g} Z_{0d}$$

DA principles of operation

- The available power gain derived as

$$G_p = \frac{1}{4} n^2 g_m^2 Z_{0g} Z_{0d}$$

- The power gain can be increased using more gain stages (n).
- In presence of T-line losses

$$G_p = \frac{1}{4} g_m^2 Z_{0g} Z_{0d} \left(\frac{e^{-n\alpha_d l_d} - e^{-n\alpha_g l_g}}{e^{(\alpha_g l_g - \alpha_d l_d)/2} - e^{-(\alpha_g l_g - \alpha_d l_d)/2}} \right)^2$$

- There is an optimum n that maximizes G_p:

$$n_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d}$$

DA principles of operation

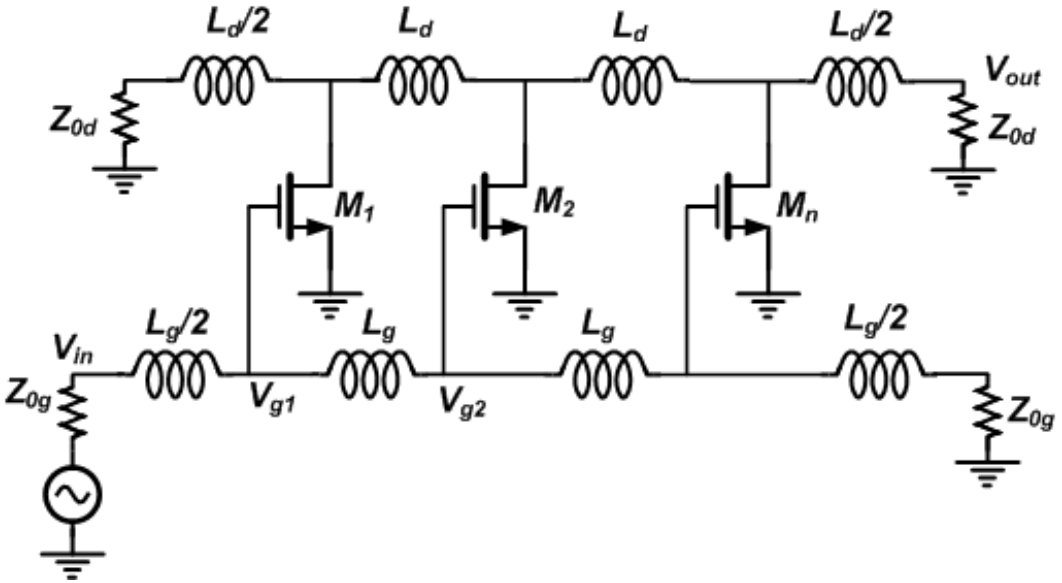
- It is desired to have T-lines with high Z_0.
- Narrow T-line: higher loss (ohmic and skin effect), electron-migration limit (~ 1mA/um^2).
- Line losses are frequency-dependent; affecting gain flatness.

DA with artificial T-lines

- Image impedance for artificial T-line:

$$Z_{i\pi} = \sqrt{\frac{L}{C}\frac{1}{1-\left(\frac{\omega}{\omega_c}\right)^2}}$$

- Line propagation factor: $\theta = 2\sin^{-1}\omega/\omega_c$
- Line cut-off frequency: $\omega_c = 2/\sqrt{LC}$



DA with artificial T-lines

- Assuming $\omega_{cg} = \omega_{cd}$ and $\theta_g = \theta_d$

$$G_p = \frac{1}{4} n^2 g_m^2 R_{0g} R_{0d} e^{-2n\alpha_g(\omega)} \frac{1}{1-(\omega/\omega_c)^2}$$

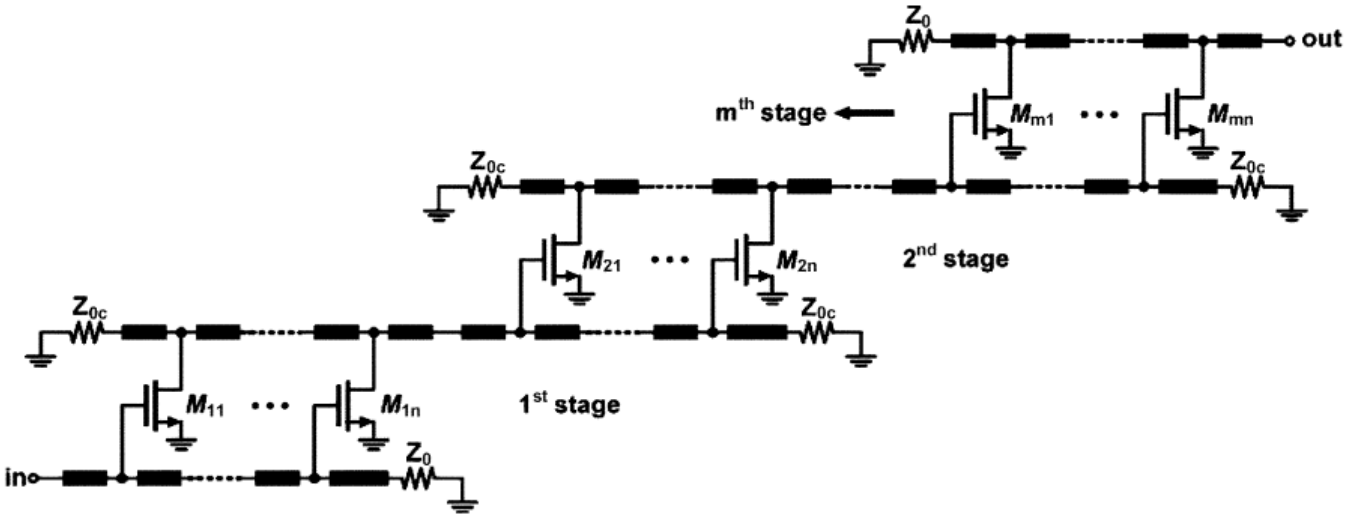
- DA bandwidth is limited by cut-off freq. of T-lines.
- DA GBW limit:

$$A_v(0)\omega_c = \frac{n g_m}{C} \cong n\omega_T$$

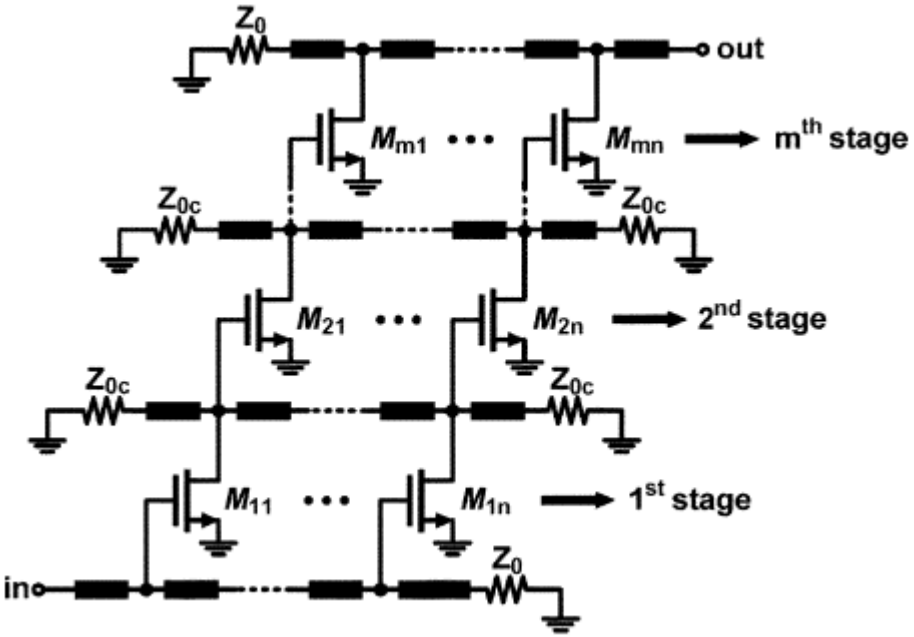
- DA frequency response exhibits undesired peaking near cut-off freq.
- Input and output lines of DA should be terminated in their image impedance.

High-gain DA architectures

Cascaded DA



Matrix DA



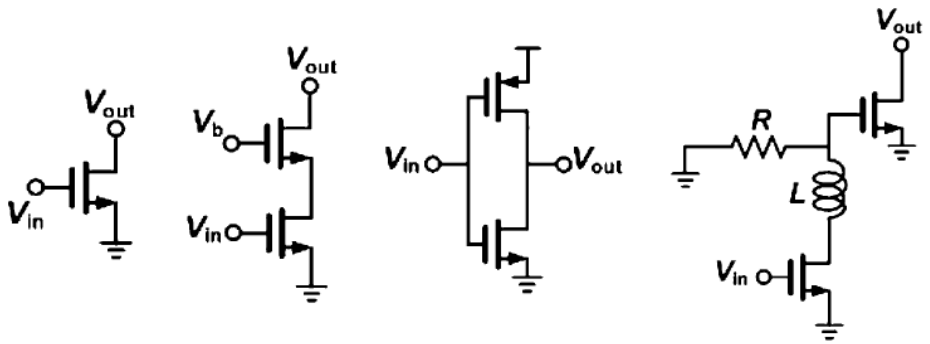
DA with improved gain stage

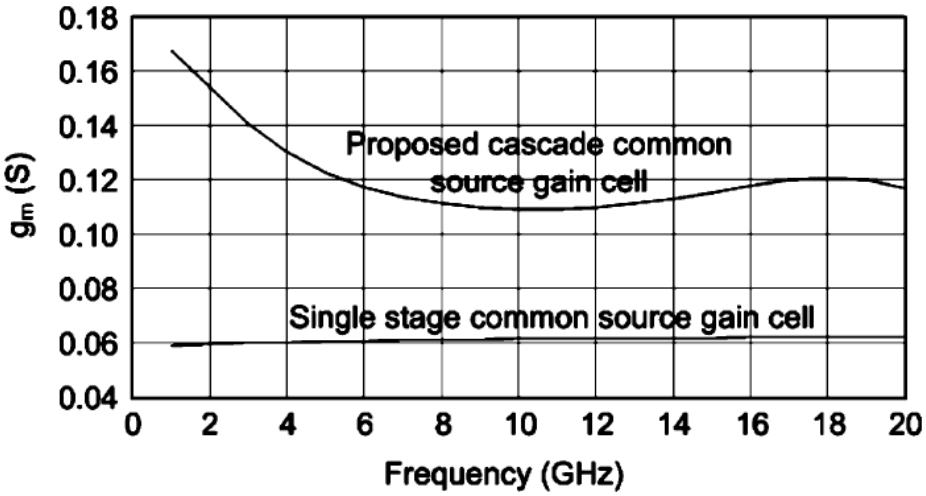
Design issues in DA gain stages:

- High G_m value is desired to enhance DA gain.
- G_m variations with freq. affect the DA gain flatness.
- BW of DA is limited by BW of G_m stages.
- Noise contribution of G_m stage should be low.
- The DA stability is compromised when using multi-stage amplifiers as gain stage.

DA with improved gain stage

- A high-gain cascode amplifier is used as gain stage (low freq. $G_m = g_{m1}g_{m2}R$)
- Values of R and L are optimized to achieve flat response.
- Average gain of 16dB is achieved over 0-11 GHz in 0.18-um CMOS.

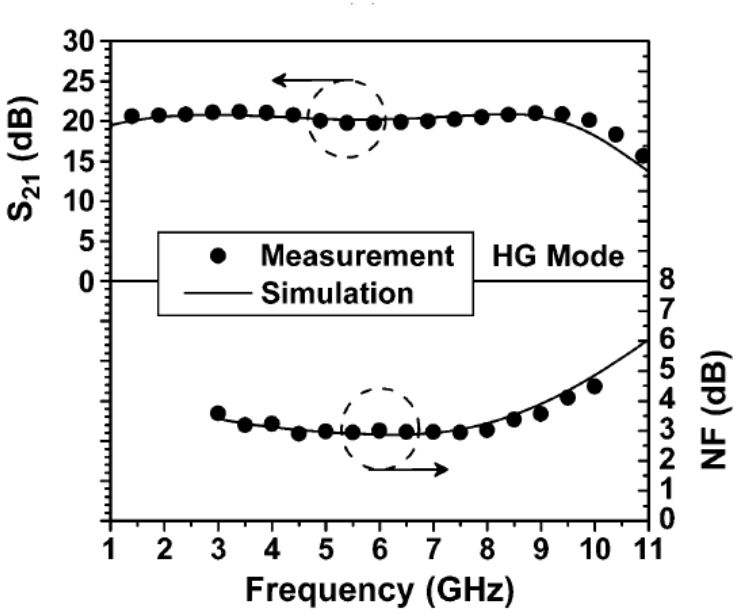


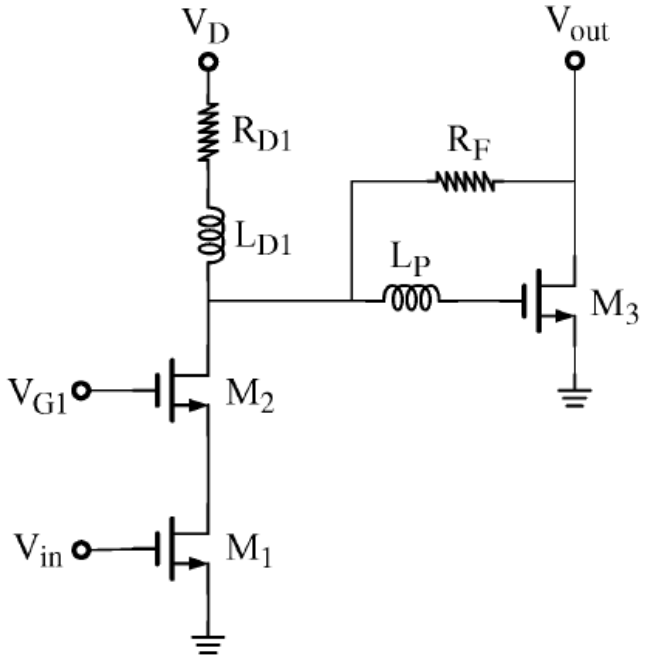


[Guan 06]

DA with inductive-peaking gain stage

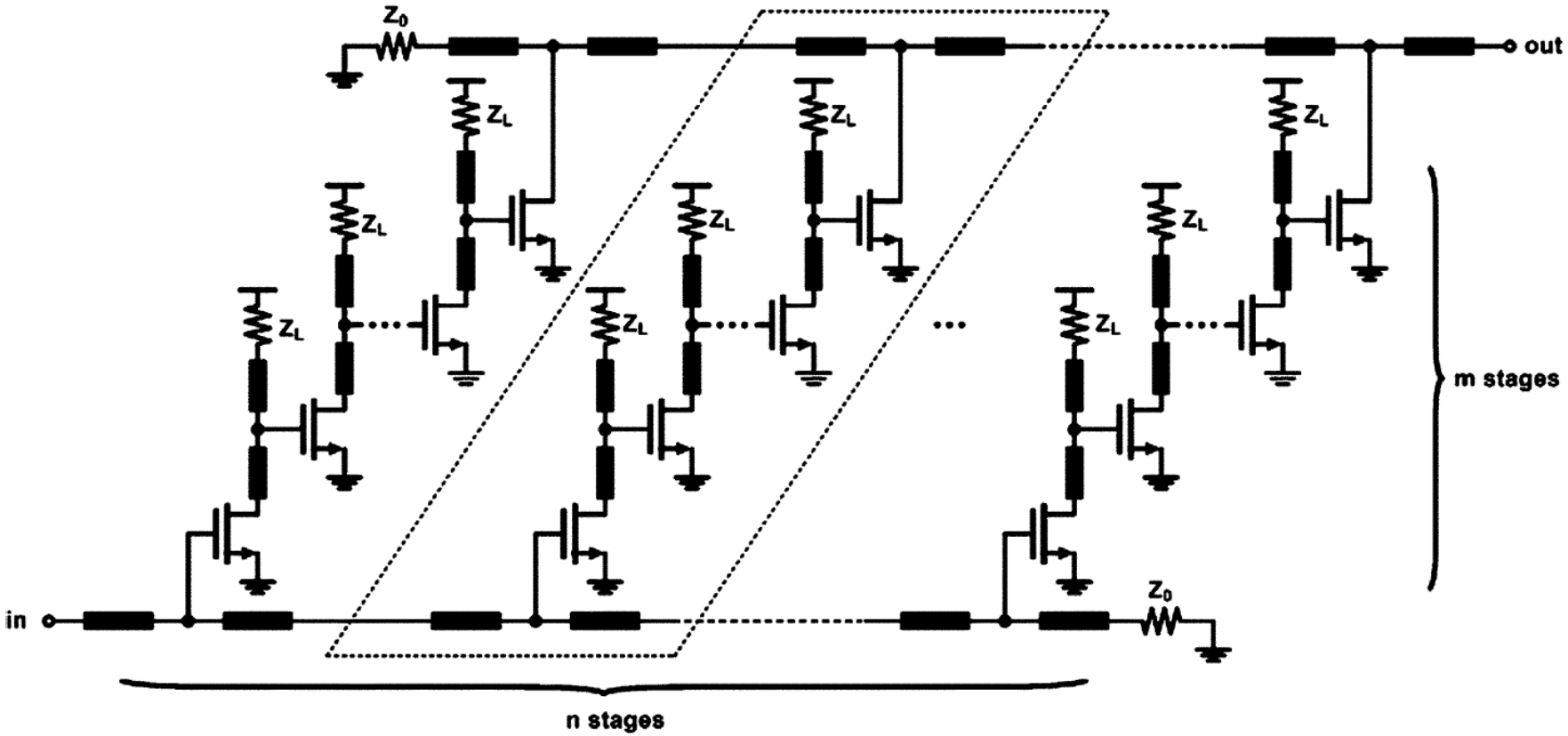
- Flat and high gain and flat and low NF are achieved by adopting a slightly under-damped Q factor for the second-order G_m freq. response.
- Two-stage DA with S_{21} > 20 dB over 3-10 GHz is designed in 0.13-um CMOS.





[Lin 11]

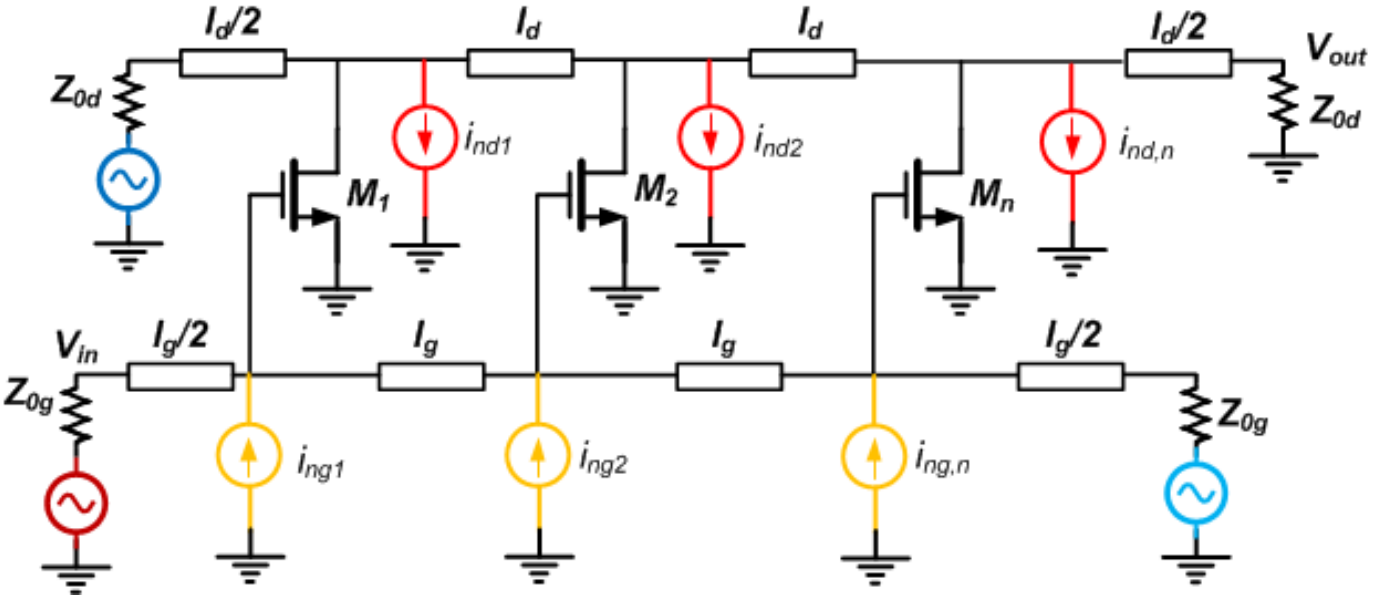
DA with cascaded gain stages



[Chien 07]

Noise in Distributed Amplifiers

- Noise sources in DA:
  - Noise from input source resistance
  - Noise from input line termination
  - Noise from output line termination
  - Noise from transistors (drain and gate current noises)



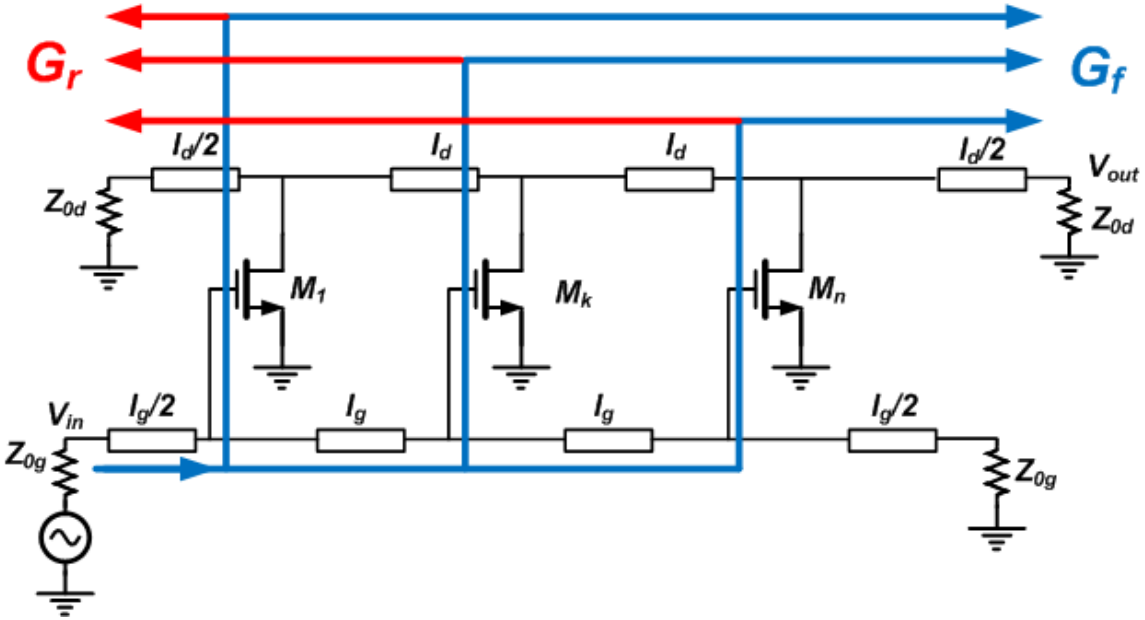
[Aitchison 85]

Noise in Distributed Amplifiers

- Concepts of forward and reverse gain:

$$G_f = \frac{1}{4} g_m^2 Z_{0g} Z_{0d} \left| \frac{\sin \frac{n}{2}(\beta_g l_g - \beta_d l_d)}{\sin \frac{1}{2}(\beta_g l_g - \beta_d l_d)} \right|^2 = \frac{1}{4} n^2 g_m^2 Z_{0g} Z_{0d} \quad (\beta_g l_g = \beta_d l_d)$$

$$G_r = \frac{1}{4} g_m^2 Z_{0g} Z_{0d} \left| \frac{\sin \frac{n}{2}(\beta_g l_g + \beta_d l_d)}{\sin \frac{1}{2}(\beta_g l_g + \beta_d l_d)} \right|^2 \quad G_r = \frac{1}{4} g_m^2 Z_{0g} Z_{0d} \left(\frac{\sin n\beta l}{\sin \beta l} \right)^2 \quad (\beta_g l_g = \beta_d l_d)$$



Noise in Distributed Amplifiers

- Noise from input source resistance appears in the output with gain of G_f.
- Noise from input line termination appears in the output with gain of G_r.
- Noise from output line termination directly appears in the output.
- Output noise due to drain current noise source in k-th transistor:

$$i_{n,out,I}(k) = \frac{1}{2} i_{nd,k} e^{-j(n-k+1)\beta_d}$$

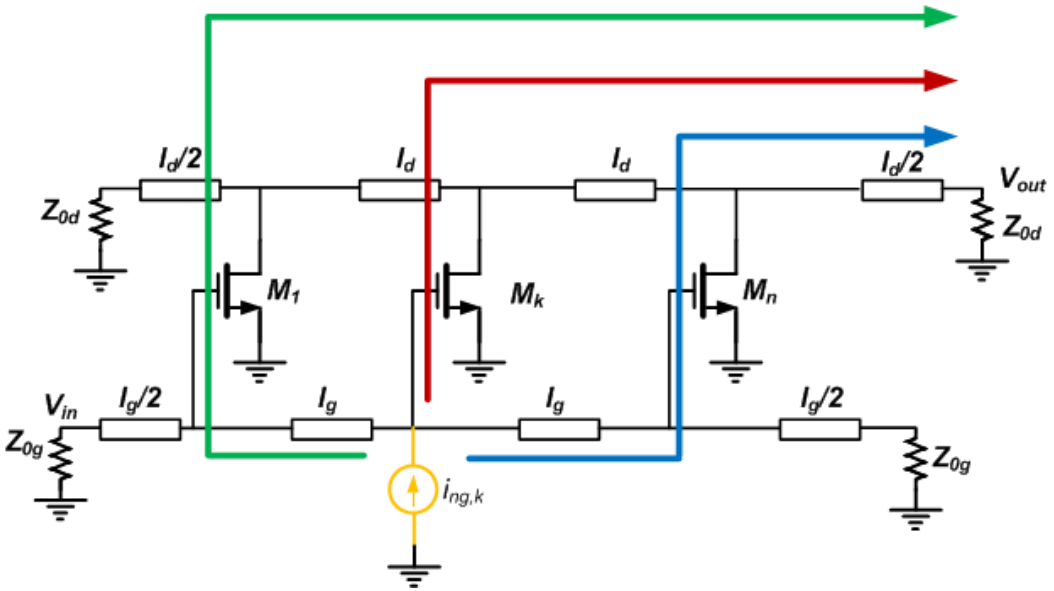
Noise due to gate current noise

- Output noise due to gate current noise in k-th transistor:
  - Forward amplification path:

$$i_{n,out,II}(k) = \frac{1}{4} g_m i_{ng,k} Z_{0g} (n-k+1) e^{-j(n-k+1)\beta}$$

  - Reverse amplification path:

$$i_{n,out,III}(k) = \frac{1}{4} g_m i_{ng,k} Z_{0g} \left[\frac{\sin(k-1)\beta}{\sin\beta} \right] e^{-j(n+1)\beta}$$



Overall noise generated by transistors

- Neglecting correlation between the drain and gate current noises, output noise power due to transistors is derived as:

$$\overline{V_{n,out}^2} = \left[\left(\frac{1}{4} g_m Z_{0g}\right)^2 \sum_{r=1}^{n} f(r,\beta)\, \overline{i_{ng}^2} + \frac{1}{4} n \overline{i_{nd}^2}\right] Z_{0d}$$

$$f(r,\beta) = (n-r+1)^2 + \left(\frac{\sin((r-1)\beta)}{\sin\beta}\right)^2 + \frac{2(n-r+1)\sin((r-1)\beta)\cos r\beta}{\sin\beta}.$$

- For FET devices:

$$\overline{i_g^2} = 4kT_0 B \frac{\omega^2 C_{gs}^2}{g_m} R \quad \text{and} \quad \overline{i_d^2} = 4kT_0 B g_m P$$

DA Noise Factor

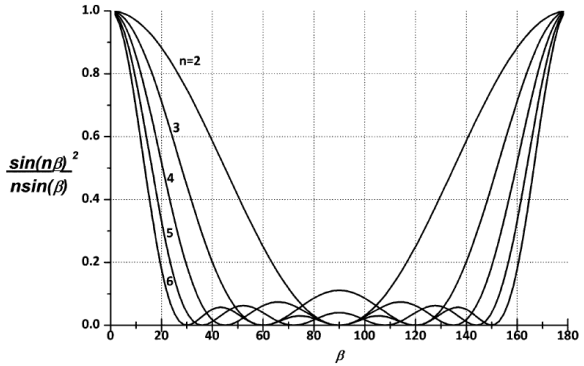
$$F = 1 + \left(\frac{\sin(n\beta)}{n\sin\beta}\right)^2 + \frac{4}{n^2 g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g}\omega^2 C_{gs}^2 R \sum_{r=1}^{n} f(r,\beta)}{n^2 g_m} + \frac{4P}{n g_m Z_{\pi g}}$$

- Noise from gate line termination is important in low and high frequencies.

$$\beta = 0\,, \pi\ (\omega = 0\,, \omega_c) \rightarrow \sin n\beta / n\sin\beta = 1$$

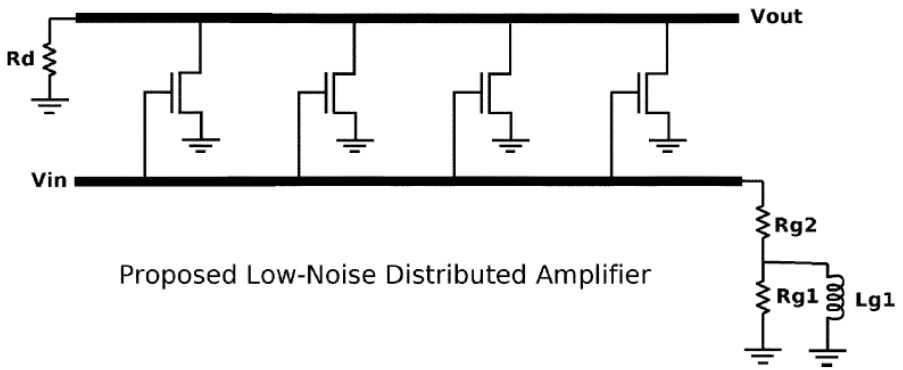
- For large values of n, noise from transistors would be dominant:

$$F = 1 + \frac{Z_{\pi g} n \omega^2 C_{gs}^2 R}{3 g_m} + \frac{4P}{n g_m Z_{\pi g}}.$$



DA noise reduction using passive termination

- The terminating resistor of the gate T-line is replaced with a resistive-inductive network.
- This terminating circuit improves the average noise:
  - It produces less thermal noise at low frequencies
  - It adds an intentional mismatch preventing the noise power to be fully transmitted to the T-line.
- Optimized values of $R_{g1,2}$ for min. noise: 20, 50 Ω

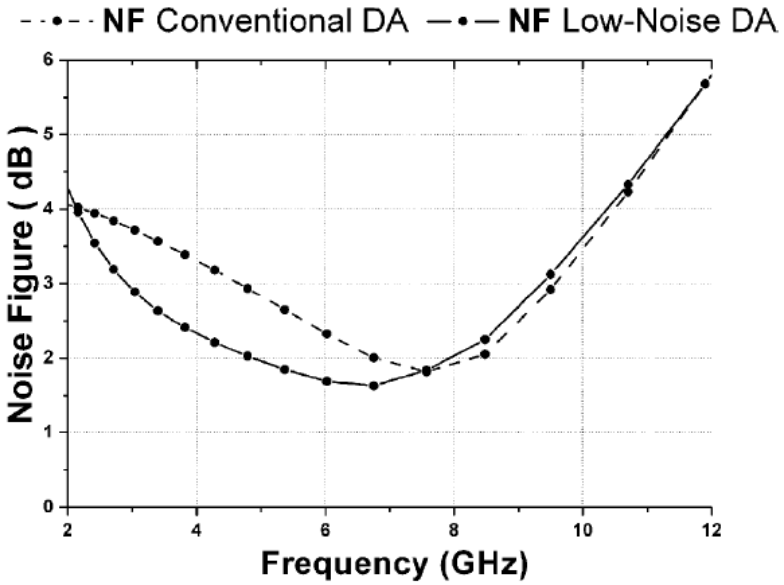


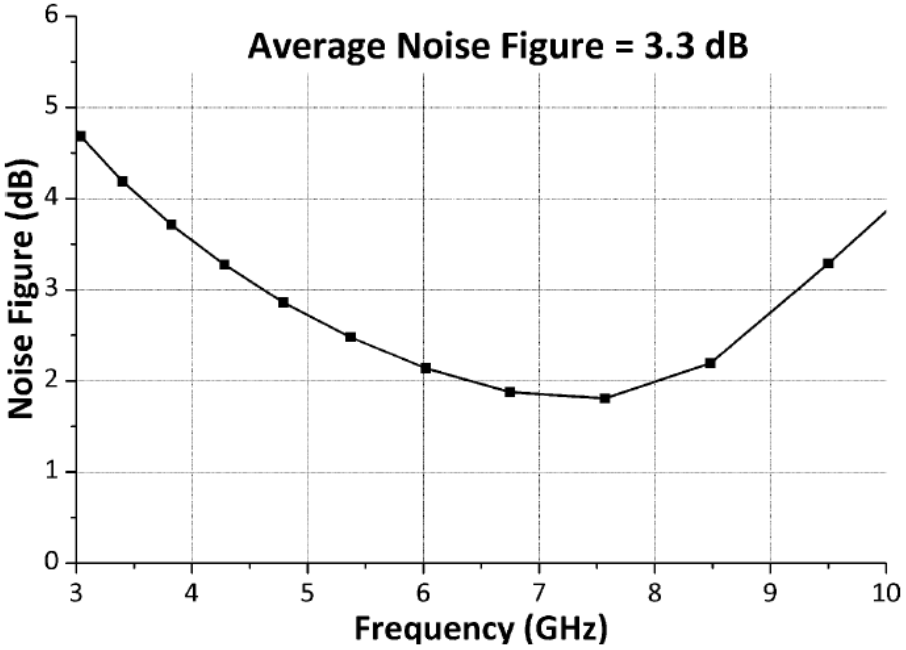
Proposed Low-Noise Distributed Amplifier

[Moez 08]

DA noise reduction using passive termination

- The lowest NF (1.8 dB) reported for DA in 0.18-um CMOS.

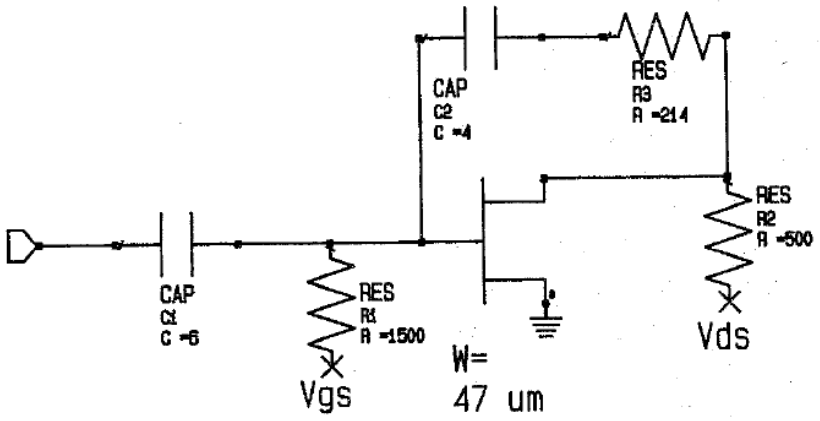


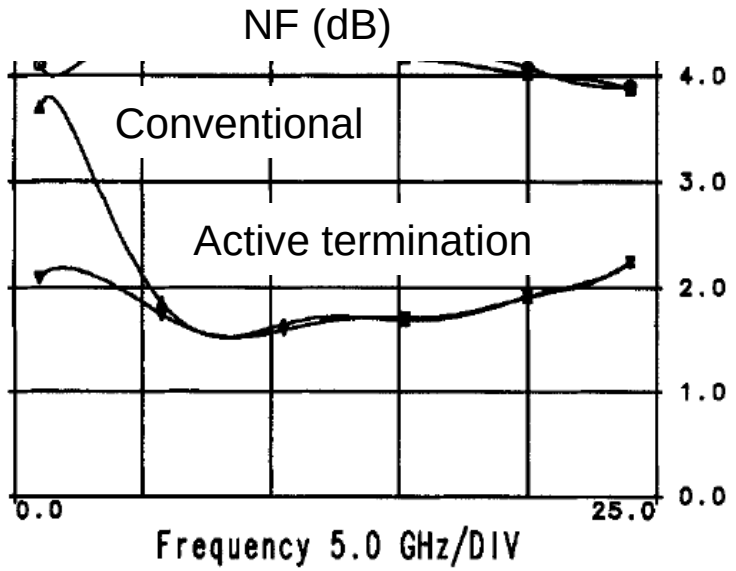


7. Measured noise figure of low-noise CMOS DA.

DA noise reduction using active termination

- A diode-connected transistor is used for termination of the input line ($R_{eq} = 1/g_m = 50\Omega$).
- A large device with low current is adopted to achieve low noise.
- NF < 2.2 dB achieved over 1-24 GHz (0.25-um pHEMT).

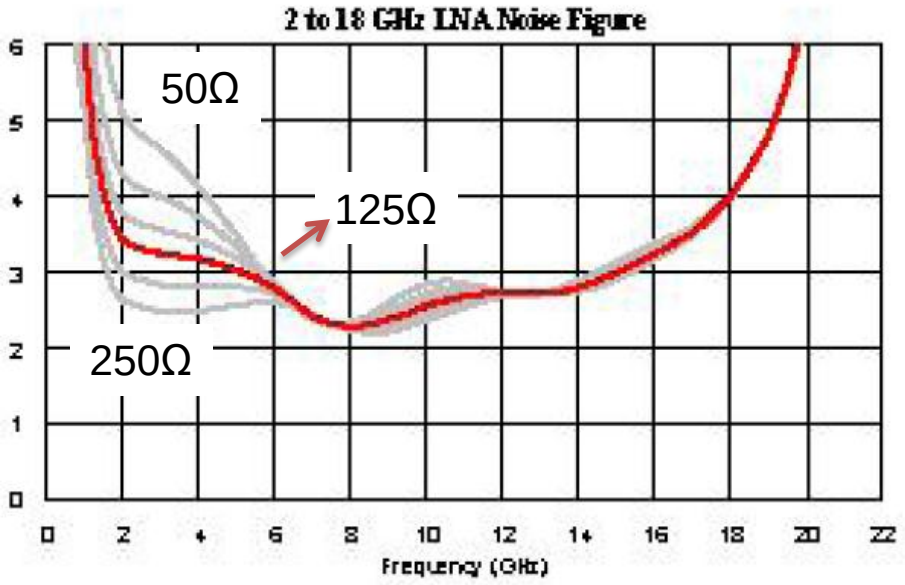


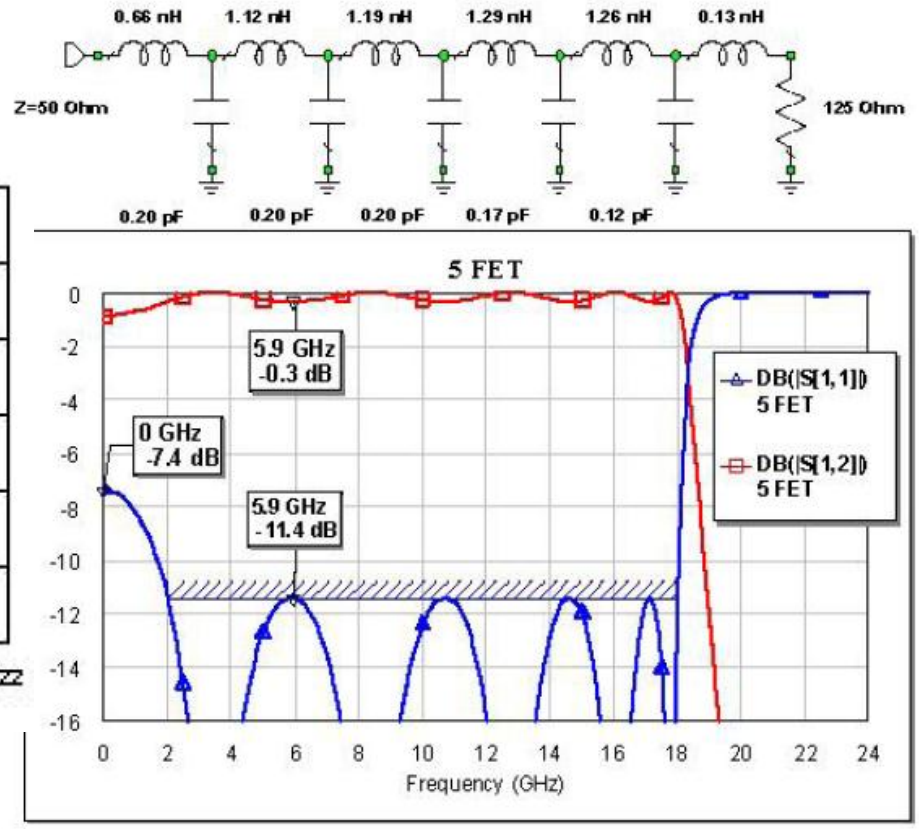


[Ikalainen 96]

DA noise reduction using high-resistance term.

- The input line terminated in a high resistance values, and designed as a transformer to provide matching.
- The max. value of termination is determined by the design bandwidth.

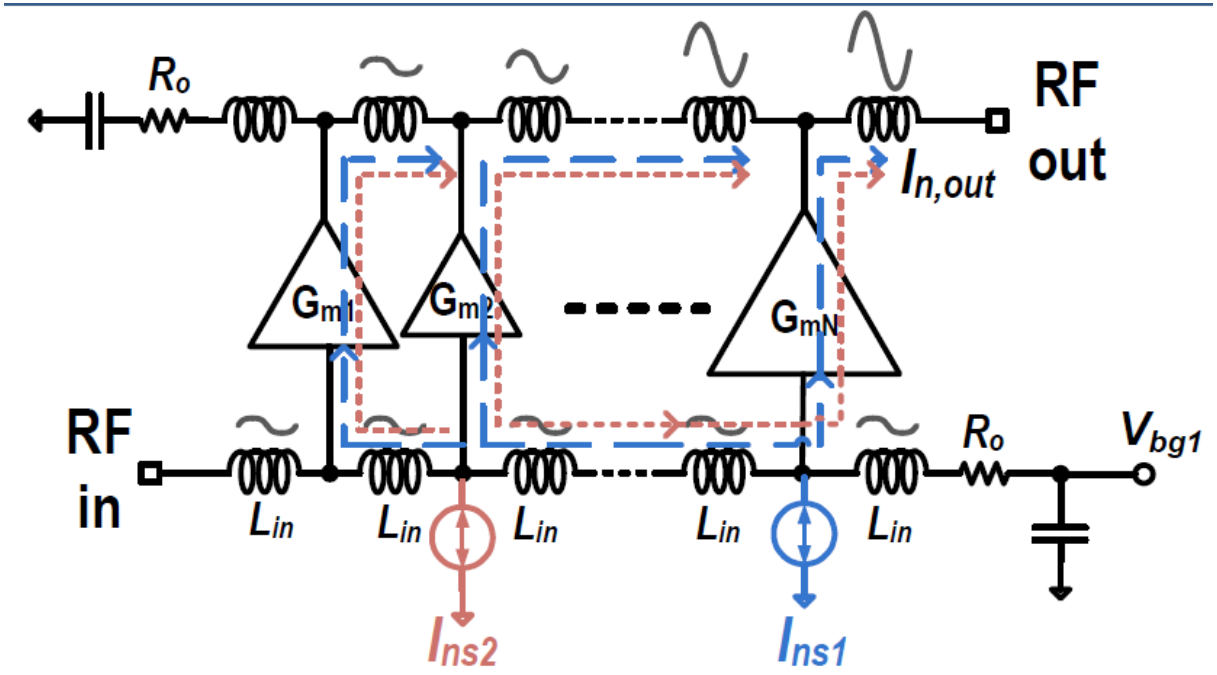




[Meharry IMS 07]

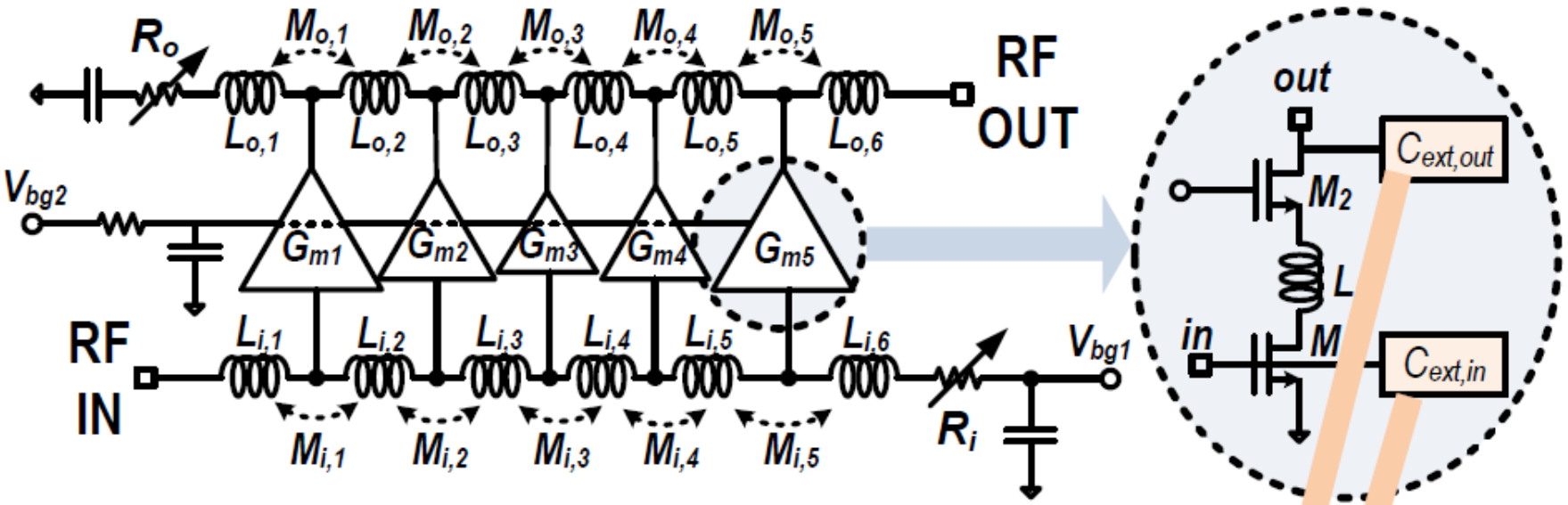
Weighted Distributed Amplification

- View the whole DA as a finite-impulse-response (FIR) system for different noise sources.
- **Design problem:** find the best weights for a given DC bias.

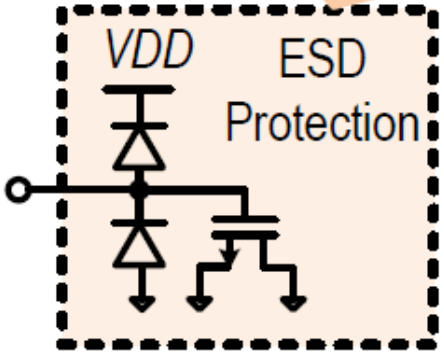


Wang and Hajimiri, ISSCC 09

Weighted Distributed Amplification



	G_{m1}	G_{m2}	G_{m3}	G_{m4}	G_{m5}
M_1, M_2 (um)	184/0.13	156/0.13	96/0.13	136/0.13	160/0.13
L_B (pH)	180	210	370	240	210
$C_{ext,in}$ (fF)	0	55	170	95	45
$C_{ext,out}$(fF)	150	180	250	205	175

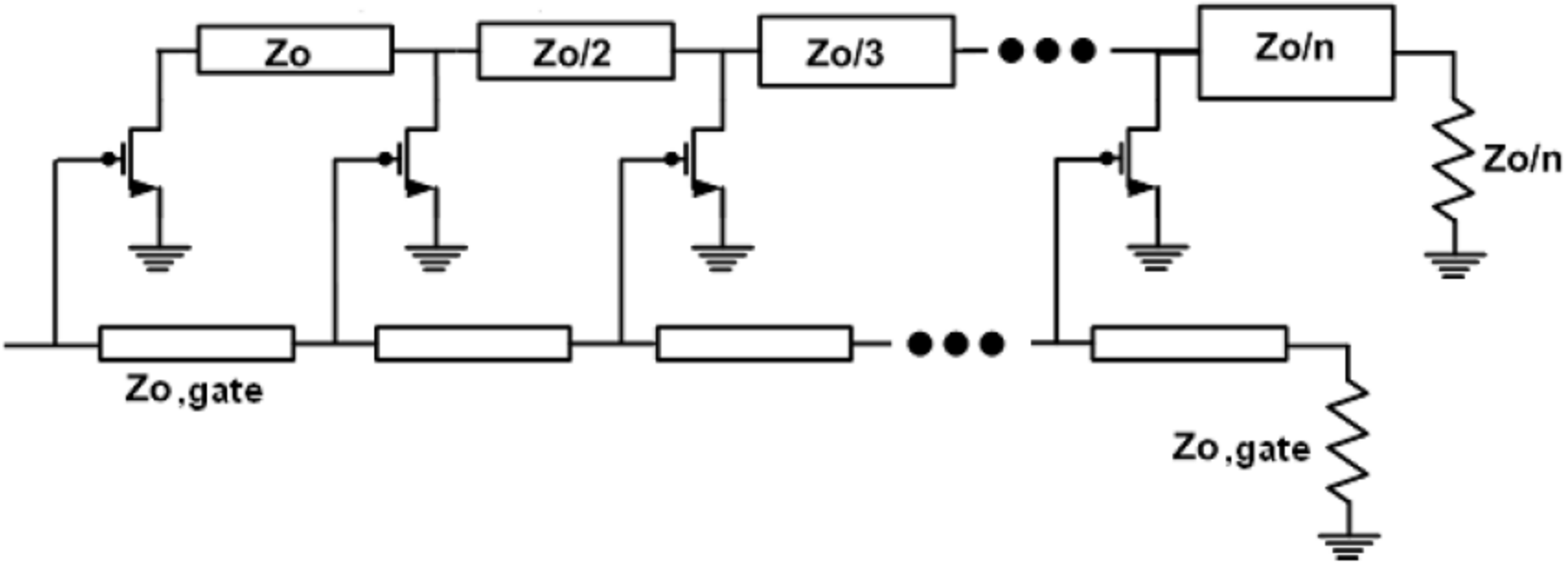


- ESD diodes can be placed at smaller gain stages.

Wang and Hajimiri, ISSCC 09

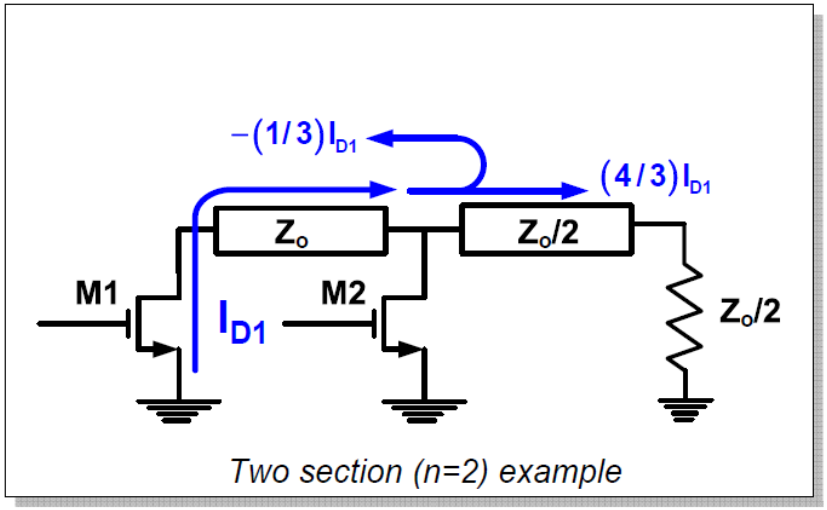
Tapered-Line DA

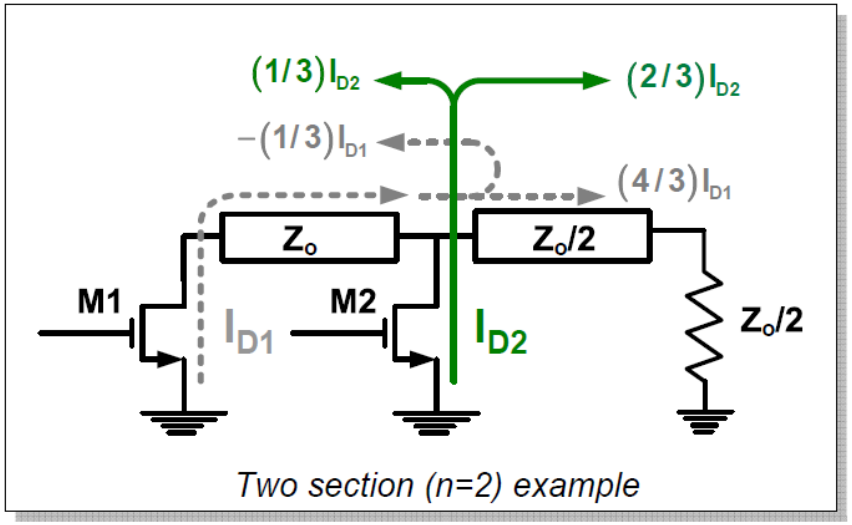
- Reverse output line termination is eliminated.



[Ginzton 48]

Tapered-Line DA





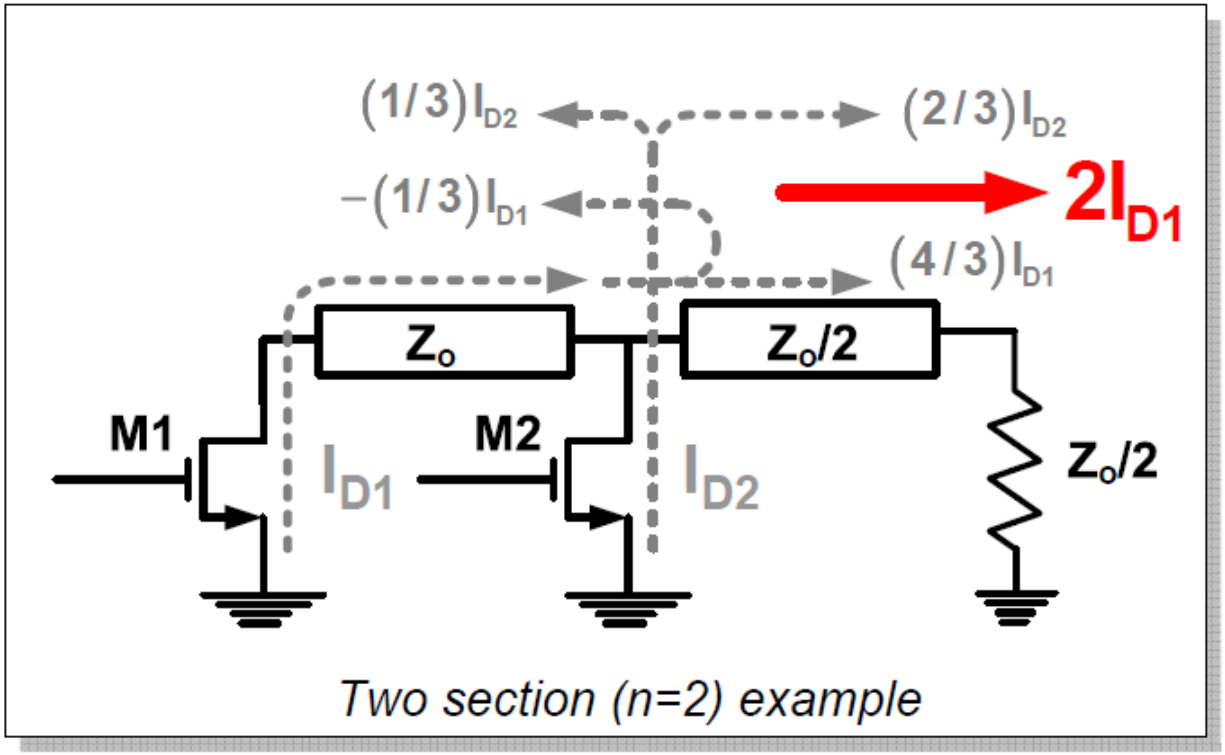
Reflection Coefficient

$$\Gamma_1 = \frac{(Z_0/2) - Z_0}{(Z_0/2) + Z_0} = -\frac{1}{3}$$

Transmission Coefficient

$$T_1 = \frac{2Z_0}{(Z_0/2) + Z_0} = \frac{4}{3}$$

Tapered-Line DA



Two section (n=2) example

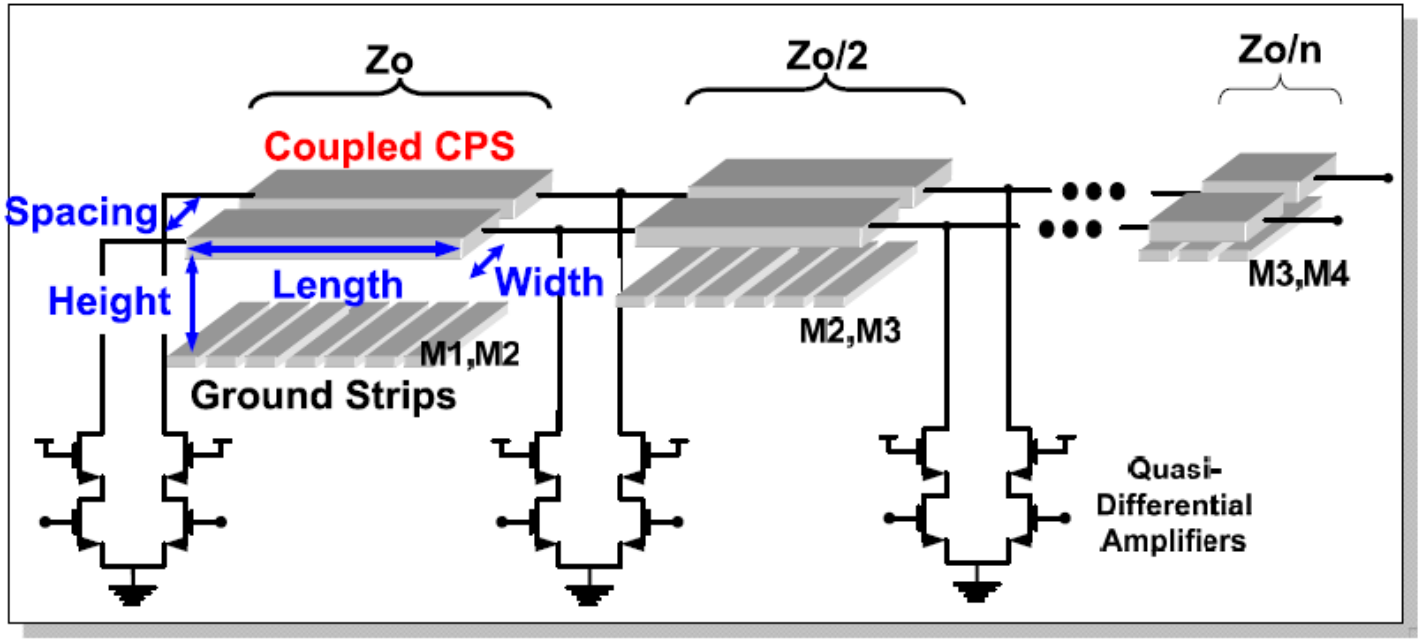
if $I_{D1} = I_{D2}$ and properly delayed:

Forward traveling currents add constructively
Reverse traveling currents cancel

Tapered-Line DA design issues

- Condition $I_{D1} = I_{D2}$ cannot be satisfied perfectly; leading to reflection in output line.
- If Z_0/n is different with load termination, a transformer would be needed at the output.
- For large values of n, very narrow or wide lines would be required in the output line sections.

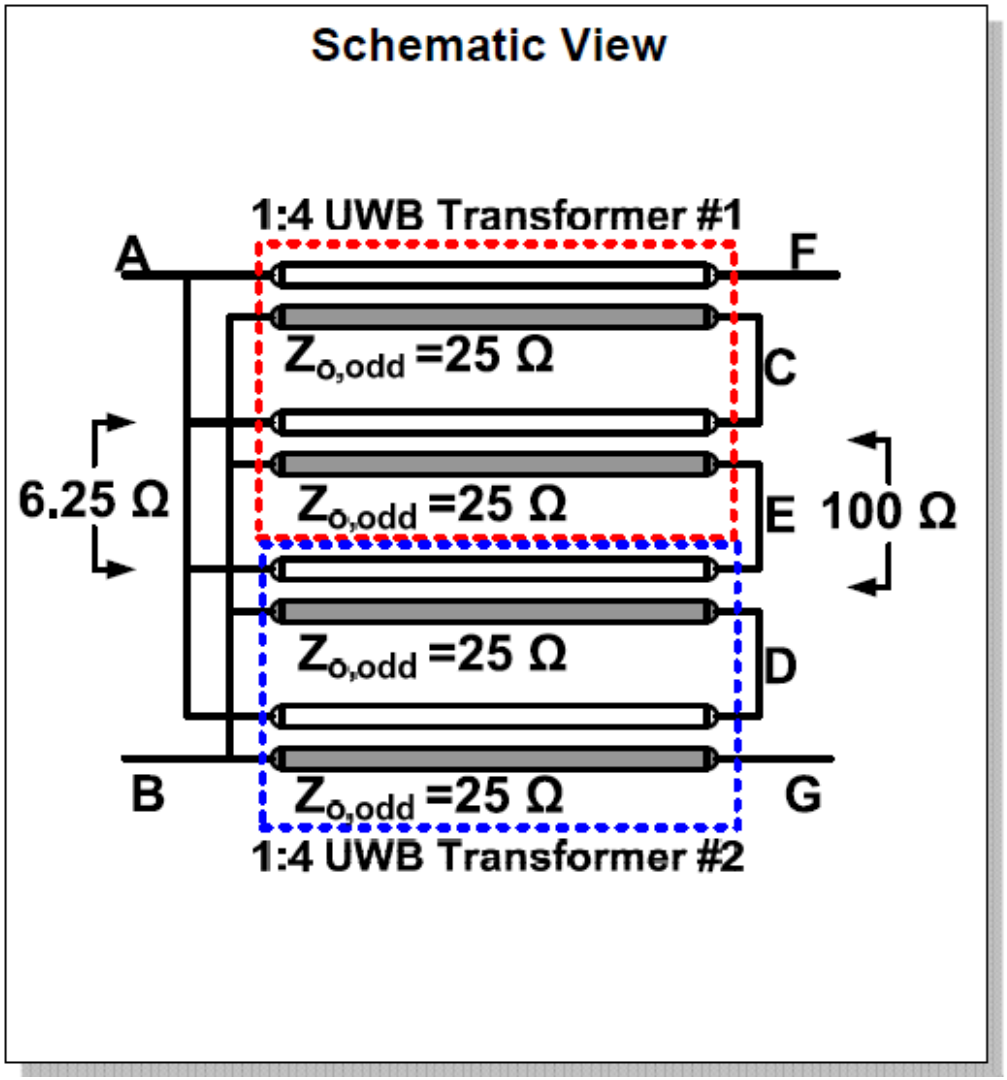
Tapered-Line DA practical example

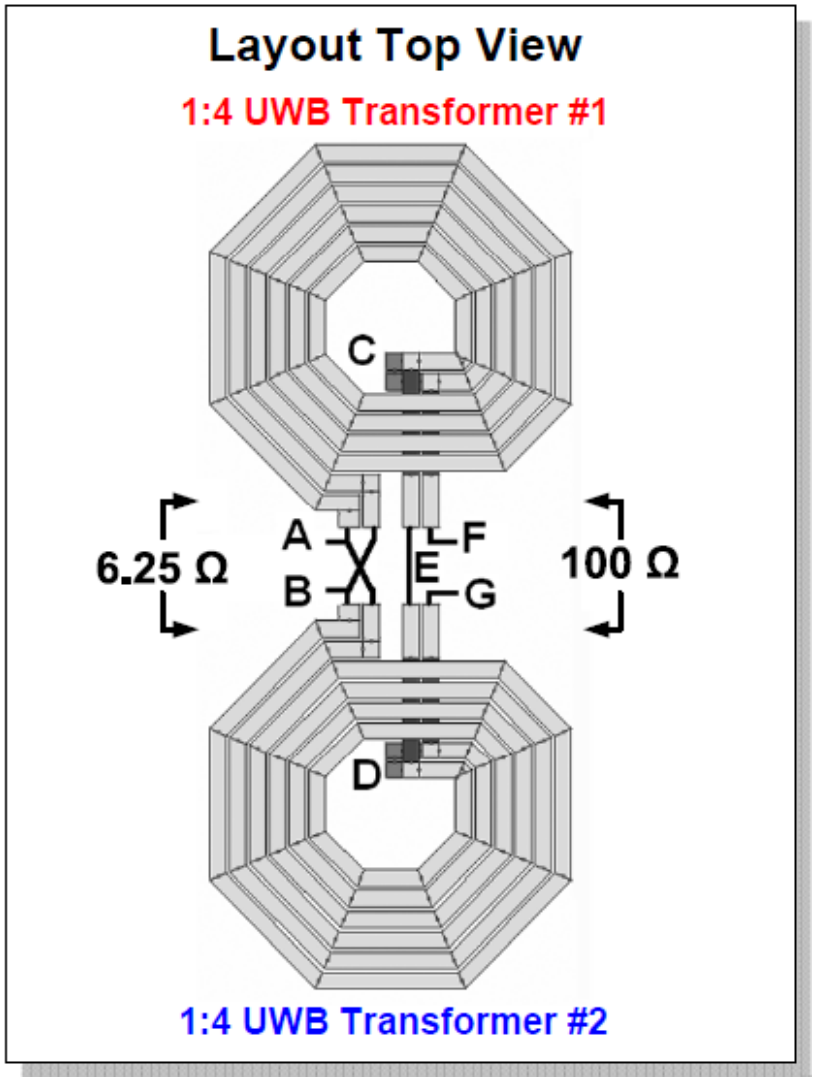


n	Section	Impedance	Length (μm)	Width (μm)	Height (μm)
1	Z_{o1}	43.75Ω	150	50	4.3
2	Z_{o2}	37.5Ω	120	50	4.3
3	Z_{o3}	31.25Ω	90	50	3.65
4	Z_{o4}	25Ω	60	50	3.65
5	Z_{o5}	18.75Ω	40	50	2.31
6	Z_{o6}	12.5Ω	35	50	2.31
7	Z_{o7}	6.25Ω	10	50	2.31

J. Roderick and H. Hashemi, ISSCC 09

Tapered-Line DA practical example

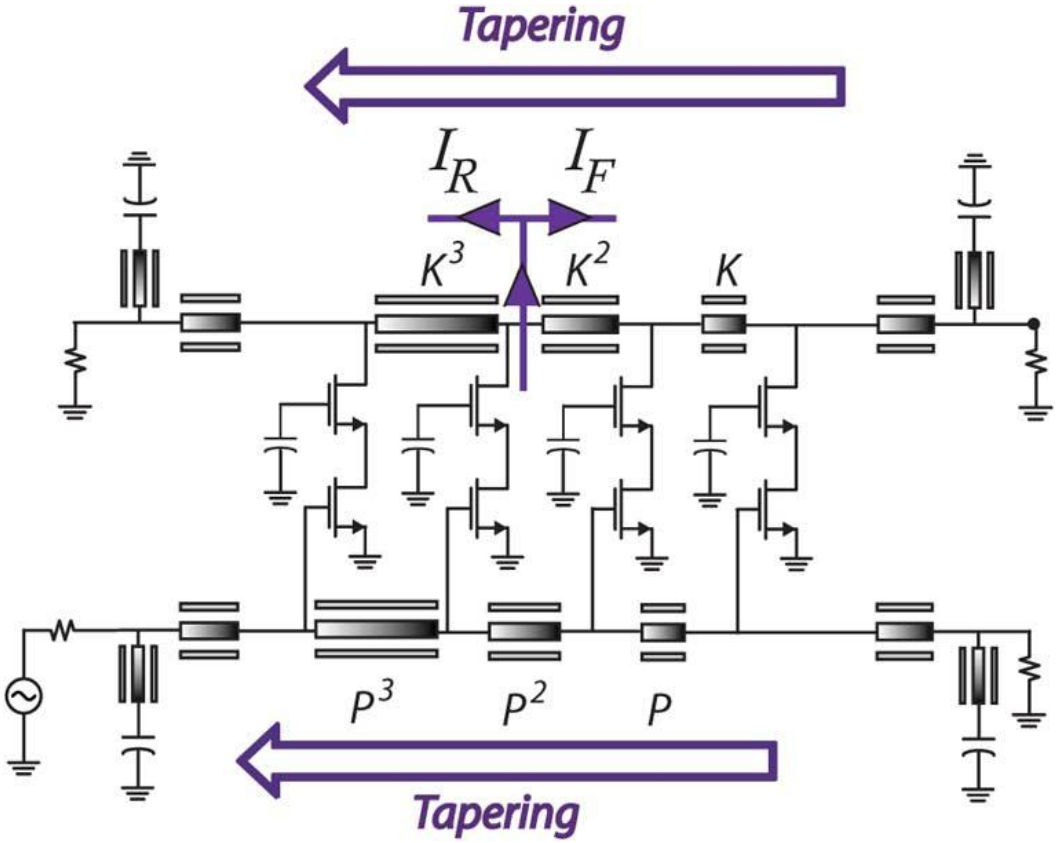




J. Roderick and H. Hashemi, ISSCC 09

Tapered DA with line termination

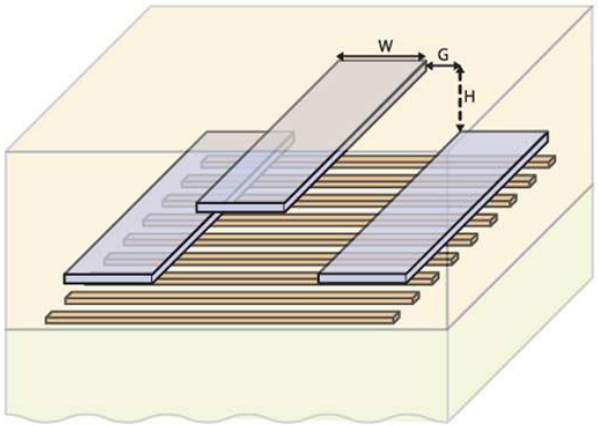
- The line impedances are tapered by scaling their lengths.
- M-derived section are employed to improve impedance matching.

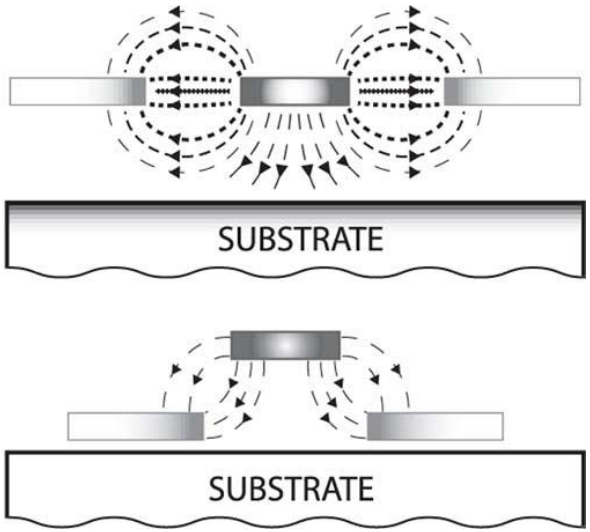


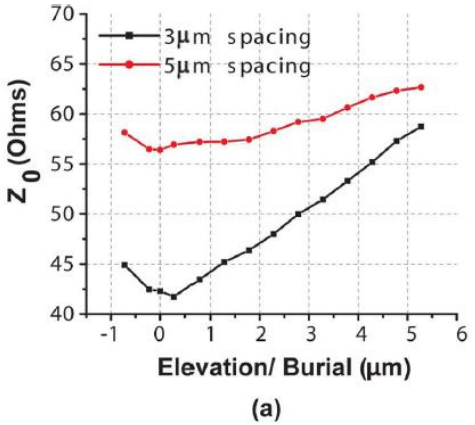
Arbabian and Niknejad, TMTT 09

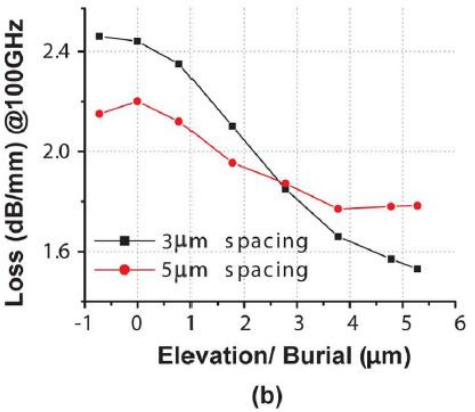
Tapered DA with line termination

- Elevated CPW with shielding is used to achieve high Z_0 values while reducing line losses.
- CPW Z_0 increases with decreasing W/(W+2G).
  - W↓ : ohmic loss↑
  - G↑ : shunt loss↑
- E-CPW improves Z_0 and loss.



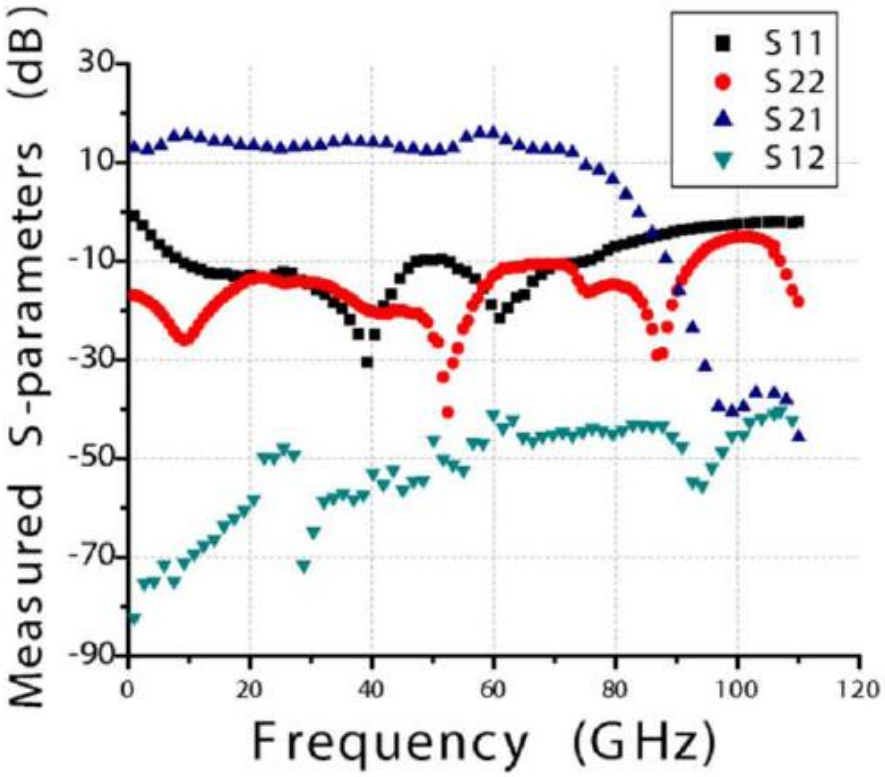






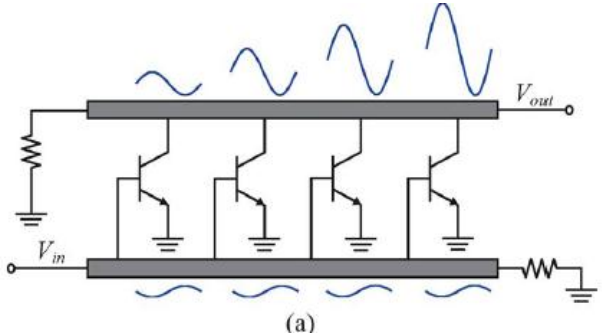
Tapered DA with line termination

- E-CPW provides Z0 over 80Ω and loss less than 0.5dB/mm over 20-60 GHz.
- Four DA stages are cascaded to improve the gain.

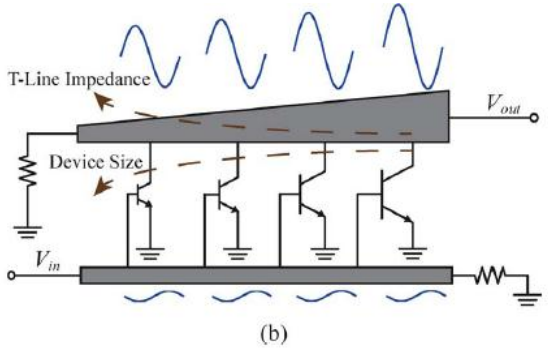


Distributed Power Amplifiers

- One major deficiency of broadband power amplifiers is their relative low efficiency.
- In a conventional distributed PA:
  - The largest voltage swing occurs at the last stage.
  - Only the last stage experiences max. allowed voltage swing when output power saturates.
  - The preceding stages never approach max. available voltage swing, hence, degrade the overall efficiency.
- The output-line impedance needs to scale up from the last stage to the first stage while the transistor size and bias current need to scale down in the same direction.



(a)

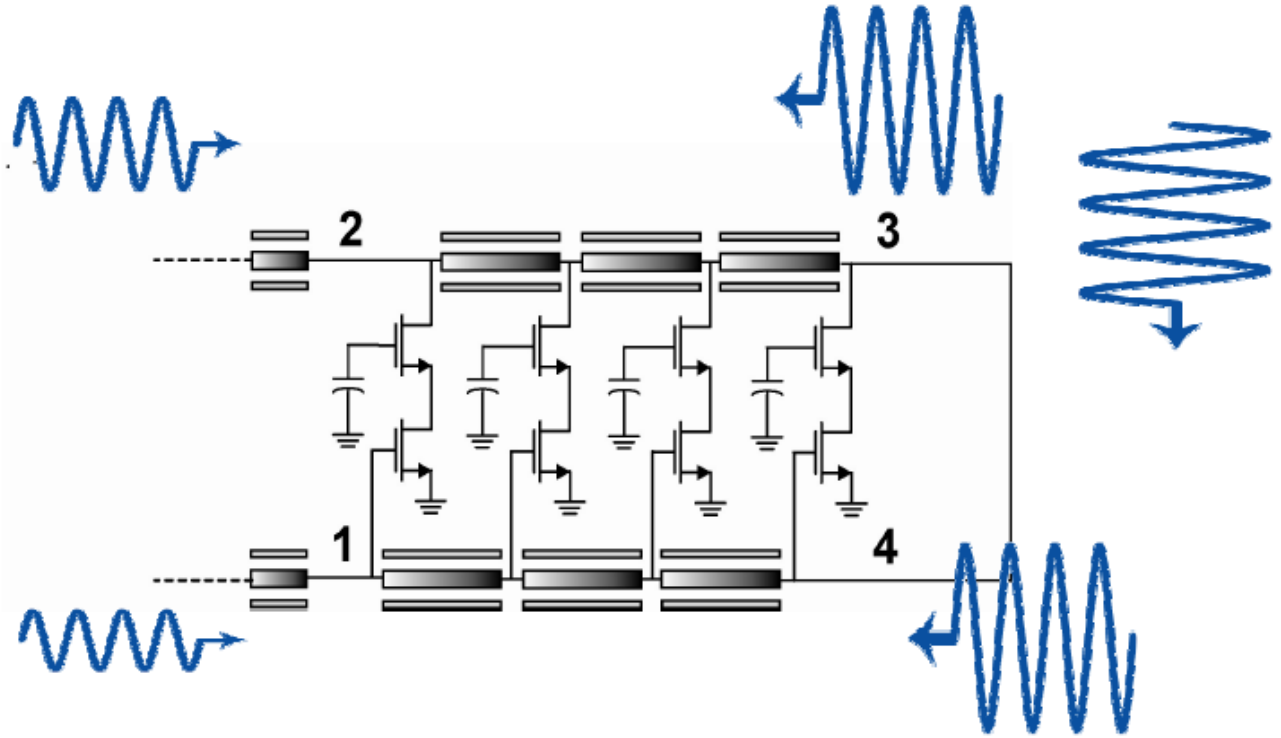


(b)

Chen and Niknejad, TMTT 11

DA with internal feedback

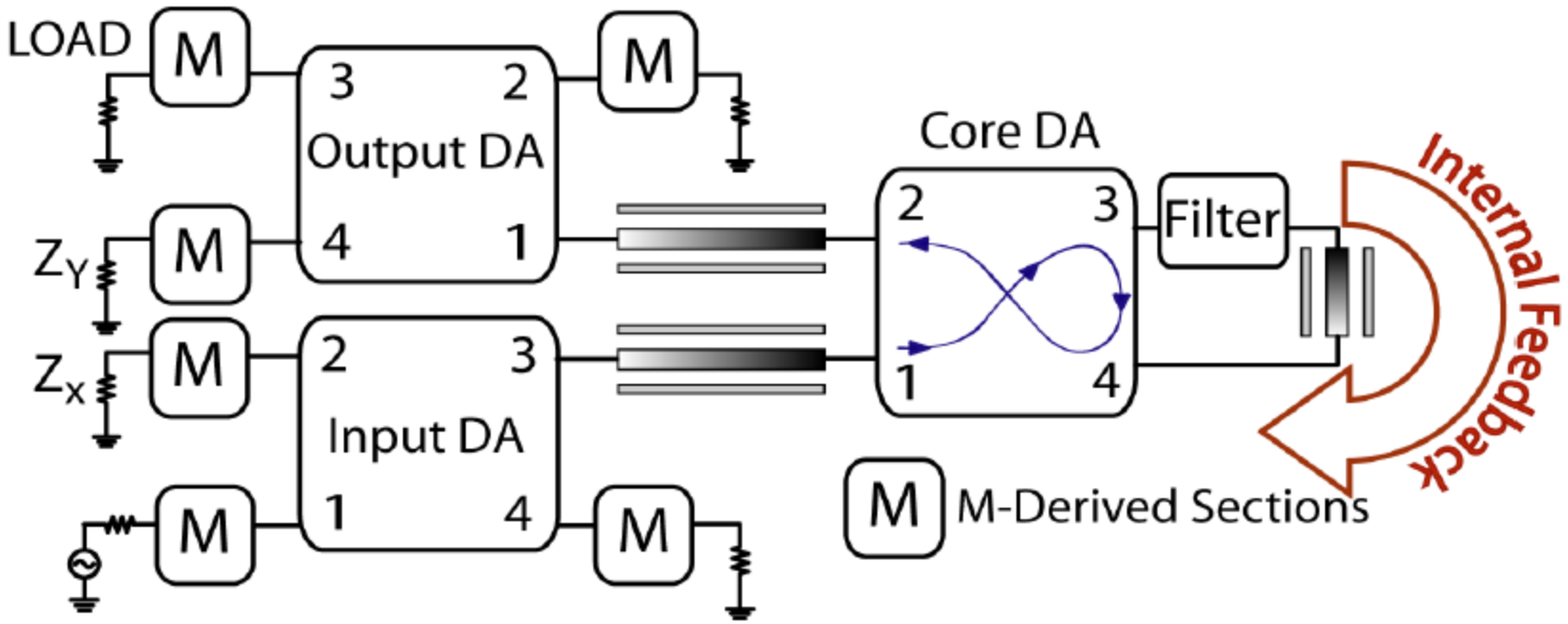
- Feedback can be employed to improve DA gain.



Arbabian and Niknejad,
ISSCC 08

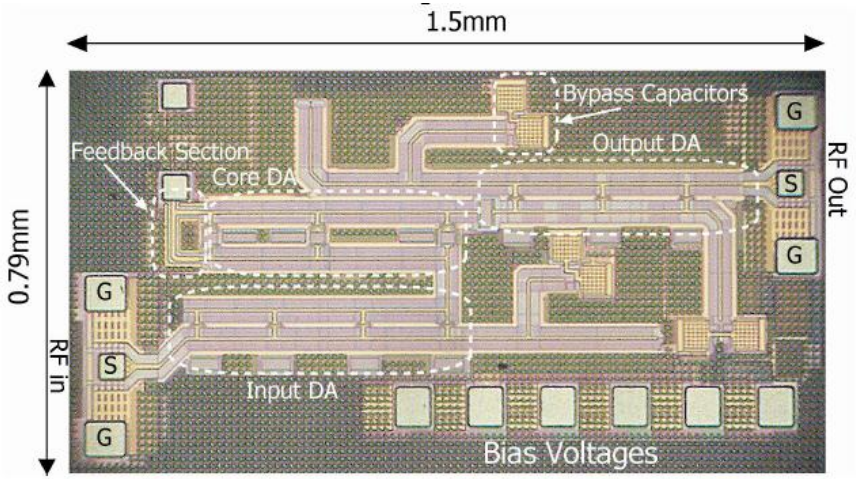
DA with internal feedback

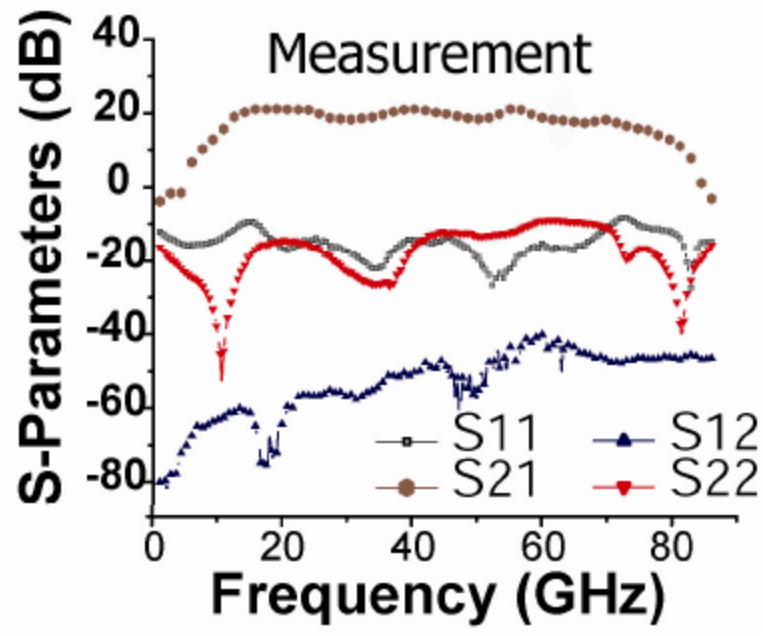
- The forward-to-reverse isolation allows stable operation.
- The input DA designed for low noise.
- The output DA designed for high output power.
- Terminations Z_x and Z_y optimized to minimize reflections.

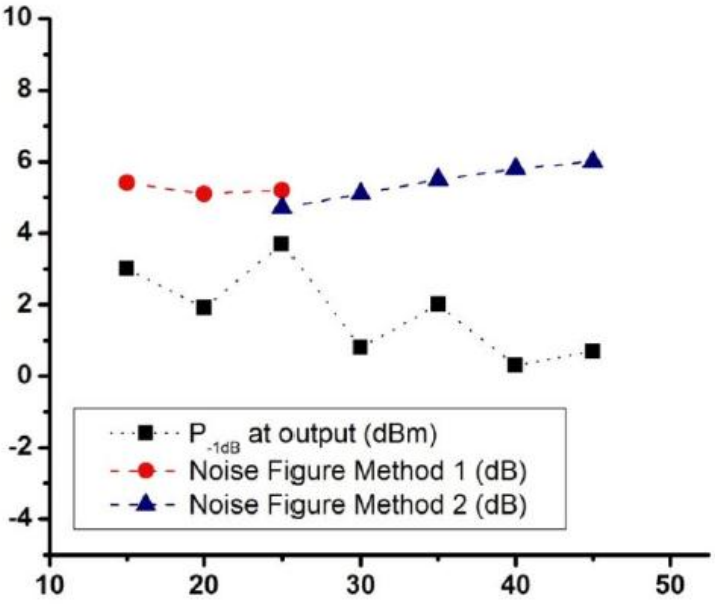


DA with internal feedback

- Gain: 19 dB
- 3-dB BW: 74 GHz
- GBW: 660 GHz
- Process: 90-nm CMOS







Loss Compensation in DAs

- A negative resistance can be inserted in the input/output of gain stages to compensate for the T-line losses.
- Design issues:
  - Implementation of broadband negative resistance
  - Flatness of freq. response
  - Stability of the DA
  - Noise contribution of negative resistance circuit

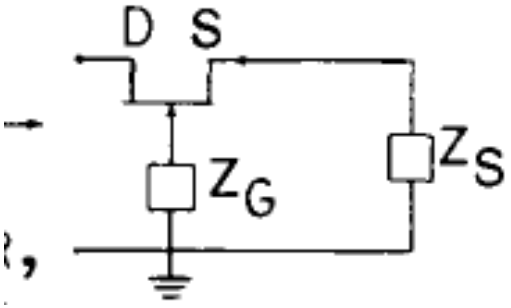
Loss Compensation in DAs

- A common-gate FET can present at its drain a broadband impedance with negative resistance.
- In low freq. Z_{nr} is high, thus has no loading on the main circuit.

$$Z_{nr}(f \to 0\ \text{Hz}) = R_{ds}(1 + g_m Z_s) + Z_s.$$

- For large Z_s values:

$$\boldsymbol{Re\{Z_{nr}\} = R_i + Z_g - \frac{g_m R_{ds}^2 C_{ds}/C_{gs}}{1 + \omega^2 C_{ds}^2 R_{ds}^2}}$$



[Deibele 89]

Loss Compensation in DAs

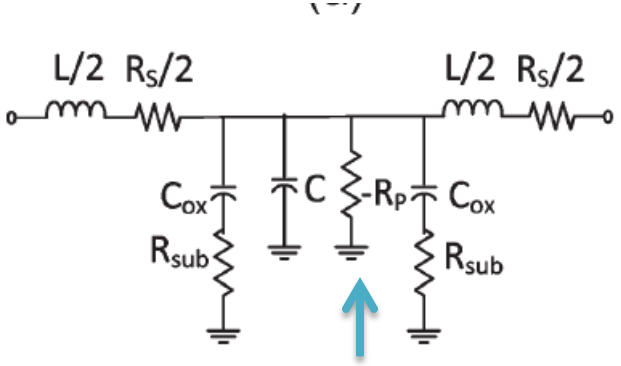
$$\gamma = \alpha + j\beta = \sqrt{(R + jwL)\left(-G + jwC + \frac{1}{R_{\text{sub}}}\right)}$$

$$= \sqrt{-\left(R\left(G - \frac{1}{R_{\text{sub}}}\right) + w^2 LC\right) + jw\left(R\left(G - \frac{1}{R_{\text{sub}}}\right) - LC\right)}.$$

$$=0 \rightarrow \quad G = \frac{LC}{R} + \frac{1}{R_{\text{sub}}}$$

- At low frequencies, the characteristic impedance of the loss-compensated TL is different from that of a lossless TL, leading to overshoot in the gain of the amplifier.

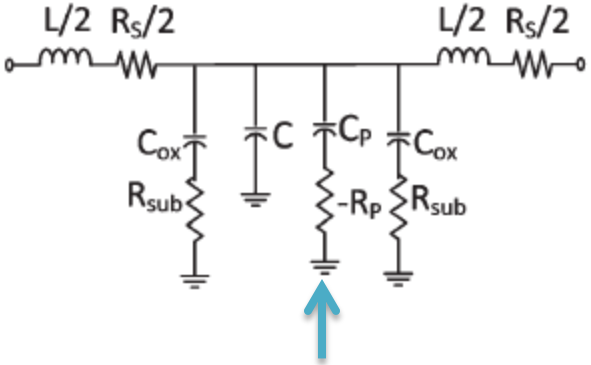
$$Z = \sqrt{\frac{R + jwL}{-G + jwC + \frac{1}{R_{\text{sub}}}}}.$$

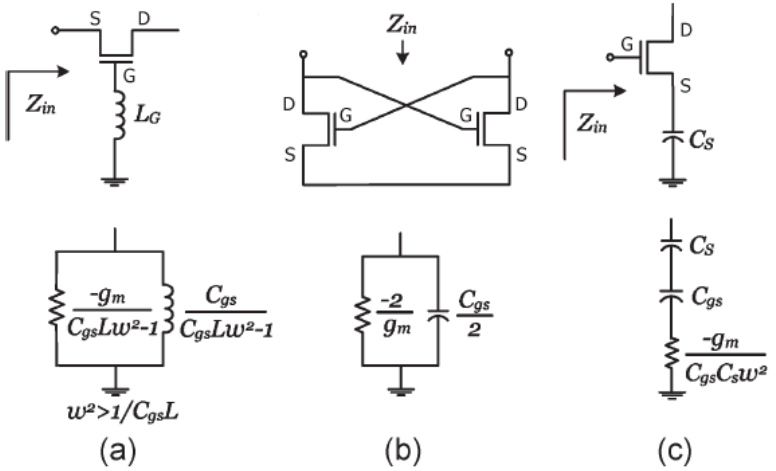


Moez ISSCC 07
Moez TCAS-II 09

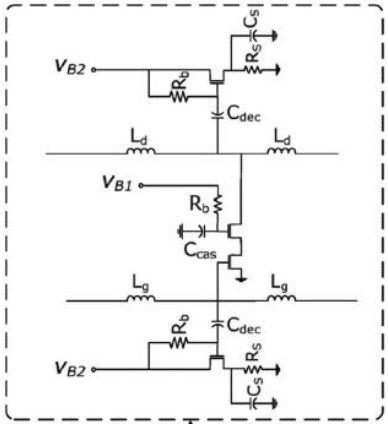
Loss Compensation in DAs

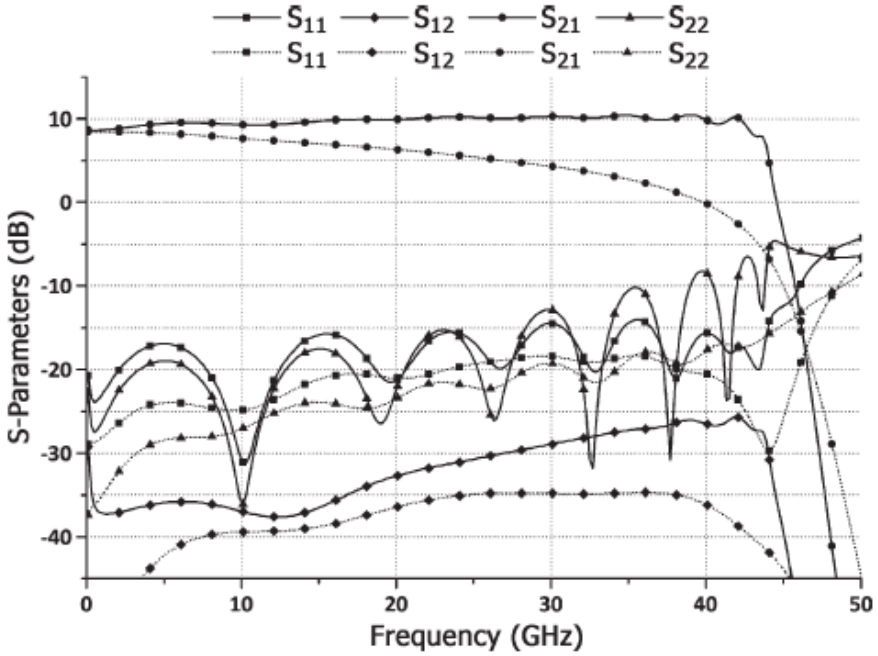
- Advantages of the modified loss compensation technique:
- 1) The negative resistance circuit does not affect the dc biasing of the circuit since it does not draw any dc current that passes through the TL components.
- 2) The negative resistance circuit does not change the characteristic impedance of the TLs at lower frequencies, and, therefore, no gain variation at low frequencies will occur.
- 3) The negative resistance is present only in the circuit at relatively higher frequencies when the effect of a series resistor on the gain of the DA is more evident and can be fully compensated.

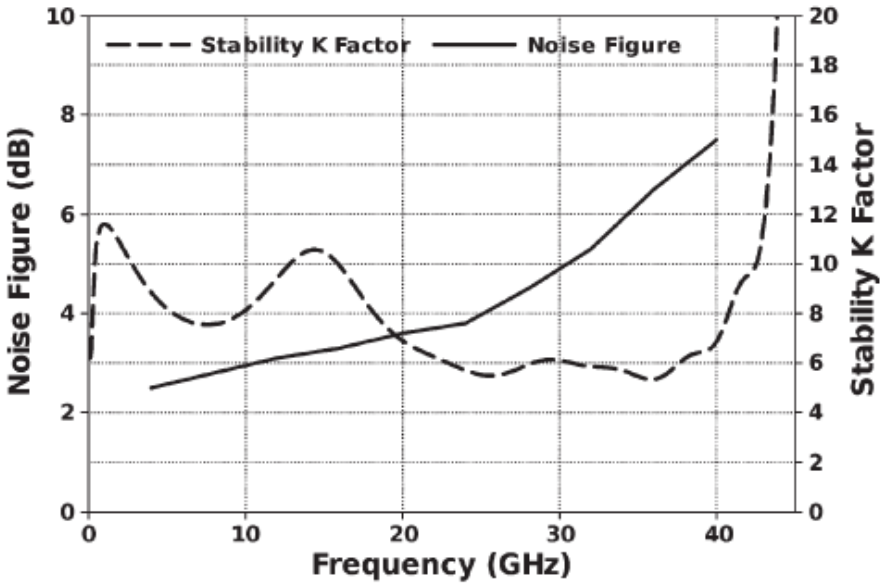




Loss Compensation in DAs

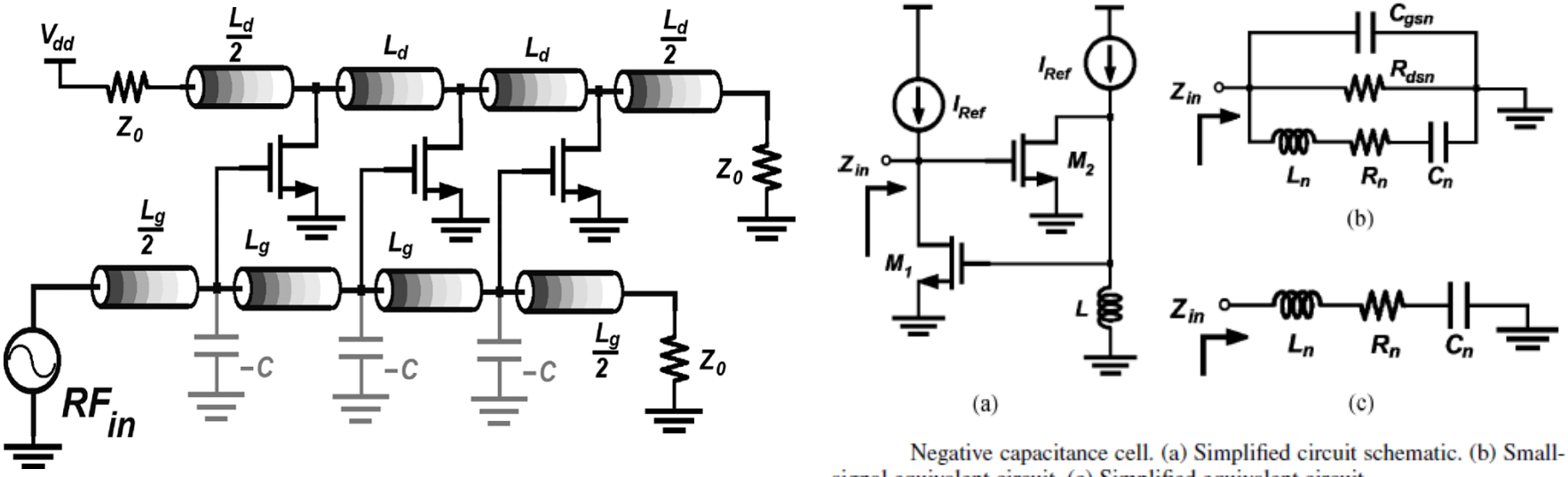






Gain-Enhanced DA using negative capacitance

- Enlarging transistors to produce sufficient g_m for a high gain increases C_{gs}, and as a result reduces cut-off freq. of input T-line, and the DA bandwidth.



Negative capacitance cell. (a) Simplified circuit schematic. (b) Small-signal equivalent circuit. (c) Simplified equivalent circuit.

$$Z_{\text{in}} = -\frac{1}{j\omega L g_{mn}^2} - j\omega\frac{C_{gsn}}{g_{mn}^2} - \frac{1}{g_{mn}^2 R_{dsn}}$$

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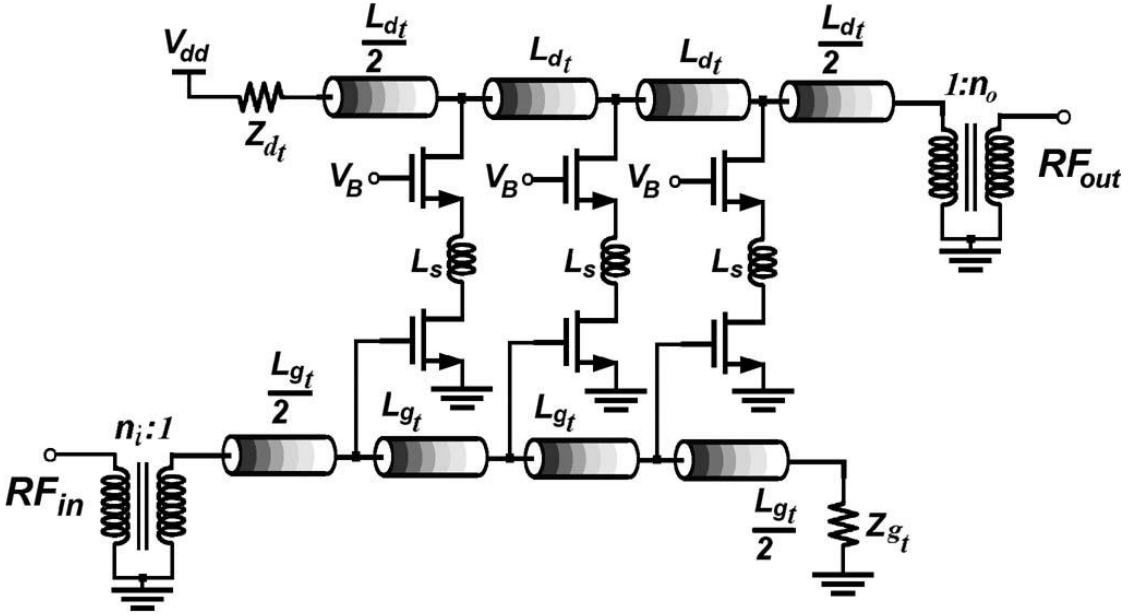
Transformer-Based DA

- For input line:

$$Z_g = \frac{Z_0}{n_i^2} \Rightarrow L_{gt} = \frac{L_g}{n_i^2}, C_{gt} = n_i^2 C_g$$

- Smaller inductors can be used to save area, and larger transistors can be used to improve gain.
- Similarly, smaller inductors can be used in output line.



Transformer-Based DA

- Broadband transformers are needed, which conventionally have low efficiency and large area.

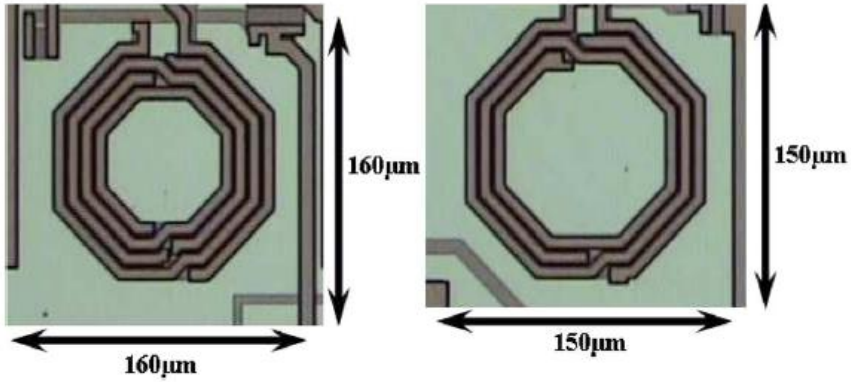


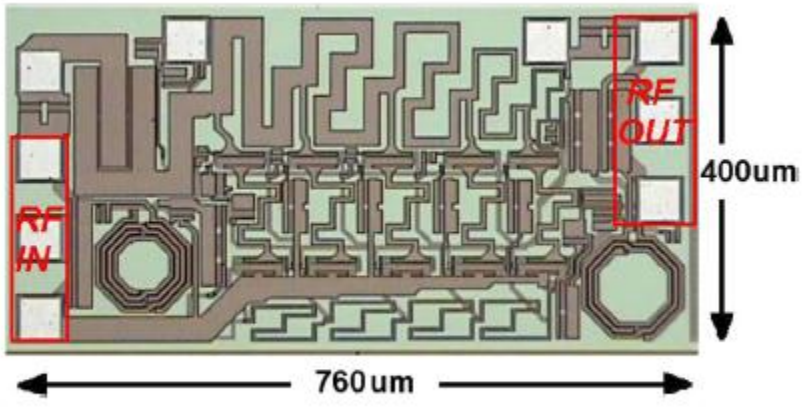
Fig. 3. Microphotograph of the input and output transformers.

PARAMETERS AND PERFORMANCE CHARACTERISTICS OF INPUT AND OUTPUT TRANSFORMERS

	Width (μm)		Space (μm)		Series Res. (Ω)		Inductance (nH)		Quality Factor		Resonance Freq. (GHz)	K_m-factor
	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.	Pri.	Sec.		
Input transformer 4:2	6	9	1.5	1.5	4.4	3.1	1.76	0.54	11	9.5	14.0	0.88
Output transformer 2:3	8	6	1	1.5	3.0	3.6	0.74	1.50	11	12	16.5	0.86

Transformer-Based DA

- The chip area is 0.31 mm^2 in 0.18-um CMOS



7. Chip microphotograph of the five-stage transformer-based DA.