Electrical Modeling and Characterization of Through Silicon via for Three-Dimensional ICs

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***Abstract*—Three-dimensional ICs provide a promising option to build high-performance compact SoCs by stacking one or more chips vertically. Through silicon vias (TSVs) form an integral component of the 3-D IC technology by enabling vertical interconnections in 3-D ICs. TSV resistance, inductance, and capacitance need to be modeled to determine their impact on the performance of a 3-D circuit. In this paper, the RLC parameters of the TSV are modeled as a function of physical parameters and material characteristics. Models are validated with the numerical simulators like Raphael and Sdevice and with experimental measurements. The TSV RLC model is applied to predict the resistance, inductance, and capacitances of small-geometry TSV architectures. Finally, this paper also proposes a simplified lumped TSV model that can be used to simulate 3-D circuits.**

***Index Terms*—Three-dimensional ICs, through silicon via (TSV), TSV lumped RLC model.**

I. Introduction

BENEFITS of 3-D integrated circuits (ICs) include improved packing density, better noise immunity, reduced power consumption, and faster speed due to reduced wire length/lower wire capacitance. In addition, 3-D ICs are promising for the heterogeneous integration of different technologies (logic, memory, RF, analog, etc.) which would enable high-performance and compact SoCs [1]. The fabrication of 3-D stacked IC (SIC) involves stacking of one or more chips, and the through silicon via (TSV) [2] constitutes a key component for interconnecting chips vertically and forms a cylindrical metal–oxide–semiconductor (MOS) capacitor with the semiconductor substrate acting as the bulk and the TSV metal acting as a gate.

The impact of TSV on the 3-D circuit performance needs to be evaluated, and there have been attempts to characterize the resistance and capacitance of TSV [3], [4]. The microwave characterization of TSV [5] and the extraction of the high-frequency electrical circuit model of TSV based on S-parameter measurements [6] have been attempted. Cheng *et al.* [3] have presented the TSV C–V characteristics but do not attempt to model the TSV. The TSV structure in [3] also involves a predominant reversed bias capacitance of the p-n junction diodes. Moreover, the TSV structure and the 3-D process used in [3] and [4] are different when compared to the TSV process [7] adopted today. Leung and Chen [5] measured the resistance and inductance of large TSV structures but do not correlate them with the physical dimensions and material characteristics. Ryu *et al.* [6] extract the resistance, inductance, and capacitance of the TSV from S-parameter measurements but the corelation to the physical dimensions and material properties of the TSV is missing. In this paper, the TSV resistance $(R_{\rm TSV})$, inductance $(L_{\rm TSV})$, and capacitance $(C_{\rm TSV})$ are modeled as a function of physical dimensions and material characteristics of the TSV. A validated lumped TSV model built using the TSV RLC parameters is then approximated to form a simple lumped TSV model, which enables fast yet accurate 3-D circuit simulations.

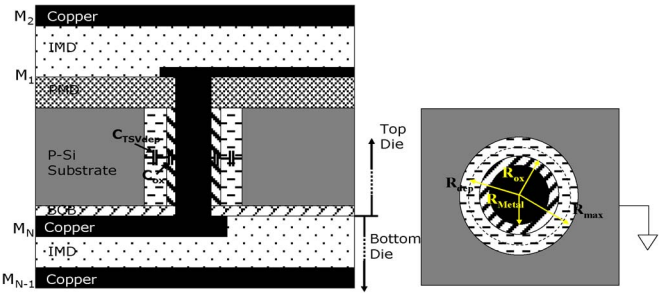

Fig. 1. TSV architecture.

First-order expressions for $R_{\rm TSV}$, $L_{\rm TSV}$, and $C_{\rm TSV}$ as a function of physical parameters and material characteristics are derived and validated with numerical simulators like Raphael [8] and Sdevice [9] in Section II. Electrical measurements performed to characterize $R_{\rm TSV}$, $L_{\rm TSV}$, and $C_{\rm TSV}$ further validate the models in Section III. Validated models are then extended to predict the RLC parameters of the future small-geometry TSV structures foreseen in ITRS [10]. A lumped model for the TSV using $R_{\rm TSV}$, $L_{\rm TSV}$, and $C_{\rm TSV}$ is proposed and further simplified in Section IV. Section V concludes this paper.

II. $R_{\rm TSV}$, $L_{\rm TSV}$, and $C_{\rm TSV}$ Modeling

In the 3-D TSV first approach [7], TSVs are fabricated after FEOL processing and before BEOL processing and enable the interconnection between the Top Metal of the bottom tier and Metal1 of the top tier, as shown in the cross section of Fig. 1. Analytical modeling starting from the basic electrodynamic principles aid in understanding the impact of physical and technological parameters on $R_{\rm TSV}$, $L_{\rm TSV}$, and $C_{\rm TSV}$.

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TABLE I
$R_{\mathrm{TSV\_DC}}$ COMPARISON BETWEEN ANALYTICAL MODEL AND RAPHAEL SIMULATIONS

TSV Diameter [um]	TSV Dielectric Thickness [nm]	TSV Length [μm]	Analytical $R_{\mathrm{TSV\_DC}}$ [mΩ]	Raphael™ Simulated $R_{\mathrm{TSV\_DC}}$ [mΩ]	% Deviation
2	50	20	118.491	119.254	0.640
2	100	20	132.023	132.872	0.639
5	50	50	44.539	44.961	0.938
5	100	50	46.414	46.853	0.939

TABLE II
EMPIRICAL L_{TSV} ESTIMATIONS

TSV Diameter [μm]	TSV Dielectric Thickness [nm]	TSV Length [μm]	Empirical L_{TSV} [pH]
2	50	20	13.827
2	100	20	14.039
5	50	20	10.185
5	100	20	10.262
5	50	50	34.262

R_{TSV} Model: The analytical expression of the dc resistance of the TSV is given by

$$R_{\mathrm{TSV\_DC}} = \frac{\rho l_{\mathrm{TSV}}}{\pi r_{\mathrm{TSV}}^2} \tag{1}$$

where ρ is the resistivity of the conducting material. r_{TSV} and l_{TSV} represent the radius and length of the TSV, respectively. The analytical model and Raphael [8] simulations show very good agreement for different TSV architectures, as shown Table I.

For high-frequency signals, however, the increase in resistance due to skin effect should be accounted. Expressions derived by Goldfarb and Pucel [11] are used to derive the $R_{\mathrm{TSV\_AC}}$ for higher frequencies. With Cu as TSV conductor, the resistivity is 16.8 n$\Omega \cdot$ m and the frequency where skin depth is equal to the radius of the TSV is estimated to be 738 MHz for a TSV with 5-μm diameter and 100-nm oxide liner thickness and 4.71 GHz for TSV with 2-μm diameter with 50-nm oxide liner thickness, respectively. As expected, resistance increase due to skin effect is quite significant for higher diameter TSV structures.

L_{TSV} Model: The partial self-inductance of the TSV depends upon the diameter and length of the TSV and is given by the following empirical expression [12]:

$$L_{\mathrm{TSV}} = \frac{\mu_o}{4\pi}\left[\begin{array}{l} 2l_{\mathrm{TSV}} \ln\left(\frac{2l_{\mathrm{TSV}}+\sqrt{r_{\mathrm{TSV}}^2+(2l_{\mathrm{TSV}})^2}}{r_{\mathrm{TSV}}}\right) \\ +\left(r_{\mathrm{TSV}} - \sqrt{r_{\mathrm{TSV}}^2+(2l_{\mathrm{TSV}})^2}\right) \end{array}\right] \tag{2}$$

where μ_o is the permeability of free space given by $4\pi \times 10^{-7}$ H/m. Empirical partial self-inductance model estimation results are shown in Table II.

For contemporary TSV architectures with 5-μm diameter and 20-μm length, L_{TSV} is estimated to be 10 pH. Inductive voltage drop ωL_{TSV} exceeds R_{TSV} only for frequencies above 3 GHz, suggesting that inductance can be ignored for clock frequencies with rise and fall times below 3 GHz.

C_{TSV} Model: An analytical expression for C_{TSV} can be obtained by solving Poisson's equation. While the planar MOS capacitor structure has been studied analytically by solving Poisson's equation [13] in a Cartesian coordinate system, the TSV MOS capacitor requires a solution of Poisson's equation in a cylindrical coordinate system. It is sufficient to solve a 1-D Poisson's equation in the radial direction, as the peripheral (Φ) and the longitudinal (z) variation in potential (Ψ) is insignificant. The 1-D Poisson's equation in cylindrical coordinate system with a p-Si substrate is given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi}{\partial r}\right) = \frac{qN_a}{\varepsilon_{\mathrm{si}}} \tag{3}$$

where q is the electron charge, N_a is the doping concentration of p-Si substrate, and $\varepsilon_{\mathrm{si}}$ is the permittivity of silicon. The boundary conditions given by the following equations suggest that the potential and the electric field (E) at the depletion radius (R_{dep}) shown in the top view of Fig. 1 is zero

$$\psi|_{R_{\mathrm{dep}}} = 0 \tag{4}$$

$$E|_{R_{\mathrm{dep}}} = \left.\frac{\partial \psi}{\partial r}\right|_{R_{\mathrm{dep}}} = 0. \tag{5}$$

This is called the partial depletion approximation that considers a depleted silicon film between $R_{\mathrm{ox}} < r < R_{\mathrm{dep}}$ near the $\mathrm{Si}-\mathrm{SiO_2}$ interface while a neutral region for $r \geq R_{\mathrm{dep}}$ in p-Si substrate, as shown in the top view of Fig. 1.

An expression for the potential variation with respect to the TSV gate voltage based on the solution of Poisson's equation and the derivation of the key MOS capacitor parameters, such as accumulation, depletion, and minimum depletion capacitance of the TSV, is elaborated in the Appendix. The nature of the TSV C–V characteristics is similar to the planar MOS capacitor such that the accumulation capacitance is the oxide capacitance given as

$$C_{\mathrm{TSVACC}} = C_{\mathrm{ox}} = \frac{2\pi\varepsilon_{\mathrm{ox}} l_{\mathrm{TSV}}}{\ln\left(\frac{R_{\mathrm{ox}}}{R_{\mathrm{Metal}}}\right)}. \tag{6}$$

As the TSV gate bias increases, the depletion capacitance acts in series with the oxide capacitance such that the effective capacitance is the series combination of the oxide and depletion capacitances. The minimum depletion capacitance is

TABLE III
C_{TSV} COMPARISON BETWEEN ANALYTICAL MODEL AND RAPHAEL SIMULATIONS

TSV Dia [um]	TSV Oxide Thickness [nm]	Na [/cm^3]	Analytical C_{ox} [fF]	Sdevice^{TM} Simulated C_{ox} [fF]	% Dev	Analytical C_{TSVMIN}[fF]	Sdevice^{TM} Simulated C_{TSVMIN}[fF]	% Dev
5	120	2e15	88.225	88.401	0.199	35.889	37.20	3.52
5	120	1e17	88.225	88.401	0.199	69.543	69.982	0.627
2	50	2e15	84.608	84.765	0.185	21.429	21.651	1.02
2	50	1e17	84.608	84.765	0.185	52.229	52.371	0.271

reached when the depletion radius reaches its maximum and is given by

$$C_{\mathrm{TSVMIN}} = \frac{C_{\mathrm{ox}} C_{\mathrm{dep\,min}}}{C_{\mathrm{ox}} + C_{\mathrm{dep\,min}}}$$

where

$$C_{\mathrm{dep\,min}} = \frac{2\pi\varepsilon_{\mathrm{si}} l_{\mathrm{TSV}}}{\ln\left(\frac{R_{\mathrm{max}}}{R_{\mathrm{ox}}}\right)}. \tag{7}$$

The accumulation and depletion capacitance expressions show that the C_{TSV} is directly proportional to the length of the TSV and inversely proportional to the TSV dielectric thickness, as expected. Moreover, R_{max} is inversely proportional to substrate doping concentration such that the depletion capacitance and threshold voltage would be higher for higher doping concentration when compared to lower doping concentration. Thus, low-doped p-Si substrates are an ideal choice to achieve minimum C_{TSV}.

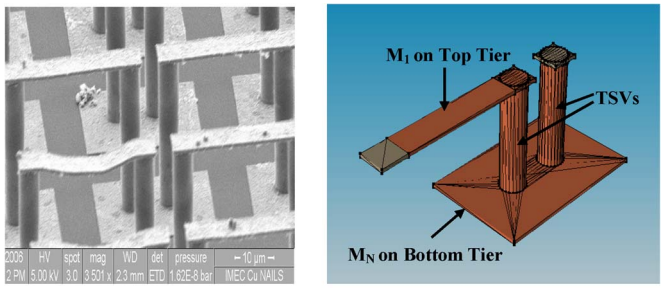
The comparison between Sdevice [9] simulations and the analytical model results for various TSV parameters is detailed in Table III. The analytical model is able to accurately predict the oxide capacitance and minimum depletion capacitance for varying TSV diameter, oxide liner thickness, and doping concentration.

R_{TSV} and C_{TSV} measurement results are shown in the next section. Experimental results are used to validate the RLC TSV models. RLC TSV models are further extended to predict the resistance, inductance, and capacitance values of future small-geometry TSVs.

III. TSV ELECTRICAL CHARACTERIZATION AND PROGNOSTICS

R_{TSV} is characterized from the resistance measurement of TSV daisy chains, as shown in Fig. 2(a). Fig. 2(b) shows a singular section of the simulated TSV daisy chain in Raphael [8]. The TSV diameter is 5 μm with 10-μm pitch while TSV length is reduced to 20 μm after wafer thinning. Raphael simulations are performed, assuming Cu resistivity to be 16.8 n$\Omega\cdot$m. Simulated resistance values are in good agreement with the measurements as shown in Table IV, suggesting the methodology can indeed be used to model the resistance of a single TSV as in Section II.

The L_{TSV} empirical model is validated with the inductance measurements performed by Leung and Chen [5] shown in Table V. It can be seen that the inductance estimations match



(a) (b)

Fig. 2. (a) SEM of 3D-SIC TSV daisy chain after etching away top substrate. (b) Section of a TSV daisy chain used for Raphael simulations.

with the inductance measurements, and the model can be used to predict the inductance of future small-geometry TSVs.

C_{TSV} is characterized by using the TSV embedded and de-embedded structures to eliminate the effect of BEOL parasitic capacitances. Fig. 3(a) shows the TSV cross section, indicating the resultant effective oxide liner thickness on the top and bottom of TSV. TSV Sdevice [9] simulation results considering $\varepsilon_{\mathrm{ox}} = 3.9$, $\phi_m = 4.7$ eV, $N_a = 2\times10^{15}/\mathrm{cm}^3$, and $t_{\mathrm{ox}} = 118.20$ nm with varying fixed oxide charges were compared with the TSV high-frequency C–V measurements, as shown in Fig. 3(b). In the desired operating voltage region from 0 to V_{dd} ($\sim$1 V), the TSV exhibits minimum depletion capacitance.

The accumulation and the minimum depletion capacitance match well with the measurements. Five-percent discrepancy in the oxide capacitance can be attributed to the reduction of oxide thickness at the bottom of the tapering TSV. In addition, the discrepancy in different C–V slopes in the depletion region can be attributed to the presence of interface states at the Si$-$SiO$_2$ interface, which have been ignored during Sdevice simulations.

The ITRS [10] predicts TSV architectures with a diameter of 1 μm and minimum TSV length of 10 μm by 2015. Figs. 4 and 5 show C_{ox} and C_{TSVMIN}, respectively, as a function of TSV diameter and oxide thicknesses with $N_a = 2\times10^{15}/\mathrm{cm}^3$ and $l_{\mathrm{TSV}} = 20$ μm. It can be seen that C_{ox} and C_{TSVMIN} increase with decreasing oxide liner thickness and increasing TSV diameter as expected. Shorter TSV length offers lower C_{TSV}, and hence, a thin wafer obtained after grinding and CMP would offer minimum capacitance compared with a thick wafer. However, processing a thin wafer increases the processing steps as the wafer has to undergo bonding and debonding with a carrier wafer during the 3-D IC fabrication.

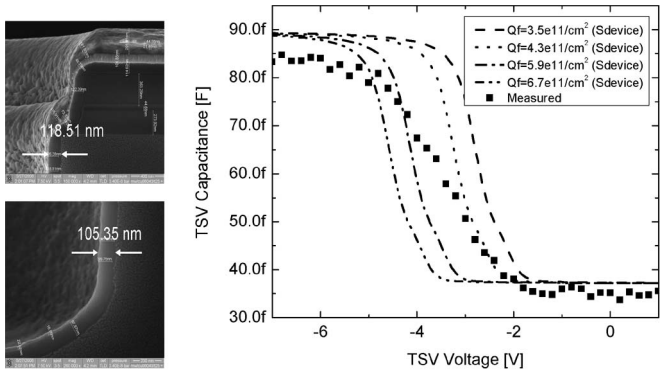
The reduction in capacitance by the depletion capacitance for varying TSV oxide thickness is shown in Fig. 6. The most

TABLE IV
RAPHAEL SIMULATION AND R_{TSV} MEASUREMENT COMPARISON

# TSVs in Daisy Chain	Measured Total Chain Resistance [Ω]	Measured Single Chain Resistance [mΩ]	Simulated Single Chain Resistance [mΩ]	% Error
8	0.704	175.881	183.587	4.382
98	10.292	210.051	183.587	12.599
998	106.222	212.870	183.587	13.756

TABLE V
L_{TSV} EMPIRICAL MODEL AND MEASUREMENT COMPARISON

TSV Diameter [μm]	TSV Length [μm]	Empirical L_{TSV} [pH]	Measured L_{TSV} [pH]	% Deviation
50	400	255.191	308.5	17.28
60	400	241.096	262.5	8.153
70	400	229.254	254.5	9.919



(a) (b)

Fig. 3. (a) Single TSV FIB image. (b). Sdevice TSV C–V simulations versus measurements.

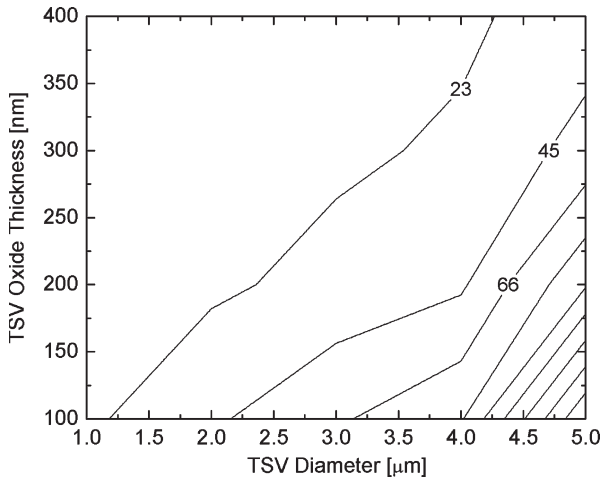


Fig. 4. C_{ox} (in femtofarads) variation with TSV diameter and oxide thickness.

effective reduction is achieved for lower oxide thicknesses. In fact, for lower oxide thickness, the oxide capacitance becomes larger and less significant in the series with the depletion capacitance. The variation of C_{TSV} with doping concentration is shown in Fig. 7. As expected, lower doping concentrations increase the depletion width and hence reduce C_{TSVMIN}, making highly resistive substrate attractive for low-capacitance TSVs.

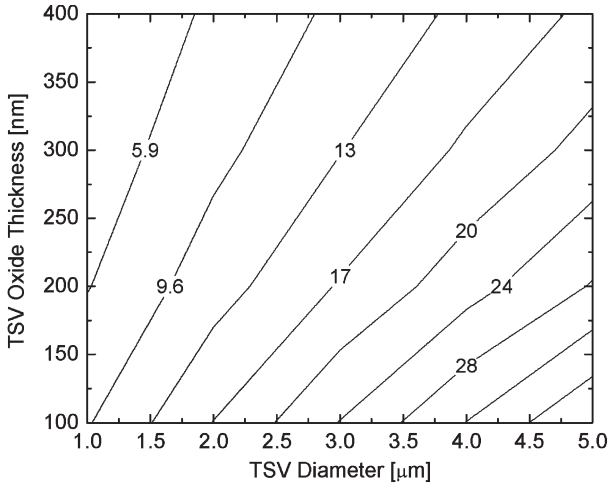


Fig. 5. C_{TSVMIN} (in femtofarads) variation with TSV diameter and oxide thickness.

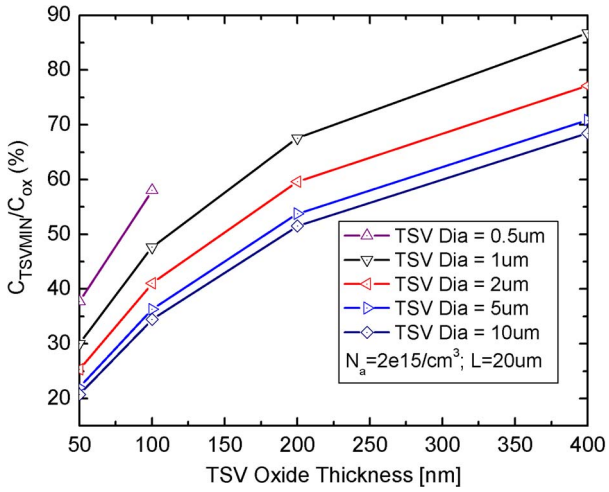


Fig. 6. C_{TSVMIN} reduction for varying TSV oxide thicknesses.

IV. LUMPED TSV MODEL

A lumped RLC model for the TSV is shown in Fig. 8(a). R_{TSV} and L_{TSV} cause the voltage drop along the interconnected nodes between Metal1 of the top tier and Top Metal of the bottom tier. C_{TSV} is connected between TSV and ground. As suggested in Section II, for the current TSV dimensions of 5-μm diameter and 20-μm length, L_{TSV} is predominant only for clock frequencies with rise and fall times above 3 GHz when $\omega L_{\mathrm{TSV}} \geq R_{\mathrm{TSV}}$. The approximate model by ignoring

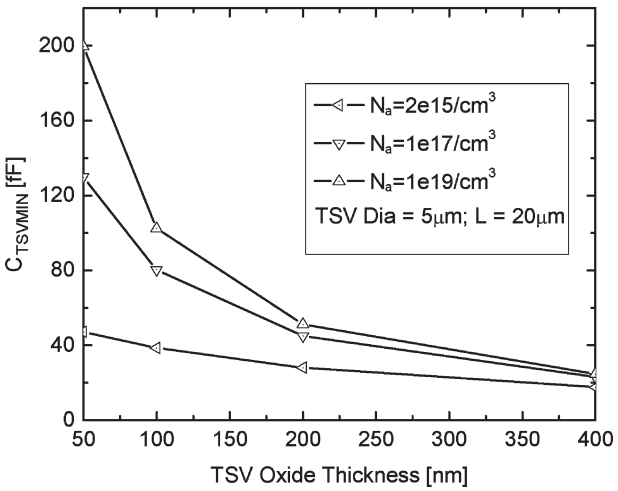


Fig. 7. C_{TSVMIN} variation with doping.

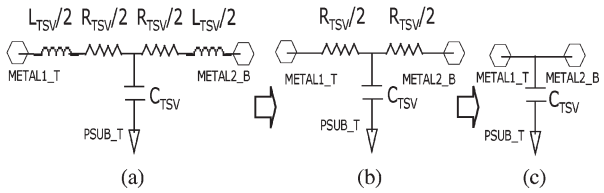


Fig. 8. (a) RLC TSV model. (b) RC TSV model. (c) C TSV model.

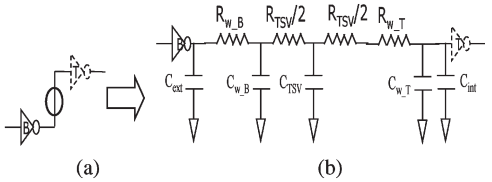


Fig. 9. (a) Bottom inverter–TSV–top inverter schematic. (b) Equivalent electrical circuit.

the inductance reduces to a simplified RC model shown in Fig. 8(b). The impact of R_{TSV} and C_{TSV} on the TSV delay can be analyzed with the help of the circuit shown in Fig. 9(a). The circuit consists of an inverter placed on the bottom tier driving an inverter on the top tier through TSV and BEOL RC loads. RC elements appearing in the signal path are shown in Fig. 9(b). C_{ext} and C_{int} indicate the output and input capacitances of the inverter. $R_{\mathrm{w\_B}}$ and $C_{\mathrm{w\_B}}$ denote the lumped BEOL load on the bottom tier while $R_{\mathrm{w\_T}}$ and $C_{\mathrm{w\_T}}$ denote the lumped BEOL load on the top tier.

The following Elmore delay expression is used to analyze the impact of R_{TSV} and C_{TSV} on the path delay:

$$\begin{aligned} tp = {} & 0.69 R_{\mathrm{dr}} C_{\mathrm{ext}} \\ & + 0.69(R_{\mathrm{dr}} + R_{\mathrm{w\_B}}) C_{\mathrm{w\_B}} \\ & + 0.69(R_{\mathrm{dr}} + R_{\mathrm{w\_B}} + 0.5 R_{\mathrm{TSV}}) C_{\mathrm{TSV}} \\ & + 0.69(R_{\mathrm{dr}} + R_{\mathrm{w\_B}} + R_{\mathrm{TSV}} + R_{\mathrm{w\_T}})(C_{\mathrm{w\_T}} + C_{\mathrm{int}}) \end{aligned} \tag{8}$$

where R_{dr} is the driving resistance of the inverter.

First-hand calculations [14] indicate that C_{int} and C_{ext} are on the order of ∼3 fF and the driving resistance of the inverter is on the order of kiloohms for 0.25-μm technology. Since $C_{\mathrm{TSV}} = 35$ fF is much larger than the C_{int} and C_{ext} values, the term $(R_{\mathrm{dr}} + R_{\mathrm{w\_B}} + 0.5\ R_{\mathrm{TSV}})C_{\mathrm{TSV}}$ has a larger weight

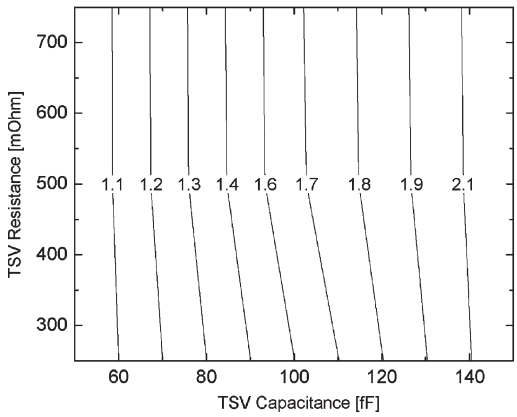


Fig. 10. RO delay (in microseconds) with varying R_{TSV} and C_{TSV}.

in determining the delay in (8). Moreover, in (8), the term R_{TSV} is always added to the driving resistance of the inverter R_{dr} and BEOL resistances $R_{\mathrm{w\_B}}$ and $R_{\mathrm{w\_T}}$. Smaller cross sections and longer lengths of BEOL metal lines provide larger resistances than estimated $R_{\mathrm{TSV}} = 18$ mΩ in contemporary TSV architecture with 5-μm TSV diameter. Hence, R_{TSV} would cause a minimal impact on the delay. A predominant impact of C_{TSV} and a reduced impact of R_{TSV} approximate the lumped TSV model, as shown in Fig. 8(c).

To corroborate the aforementioned analysis, a 41-stage ring oscillator (RO) with inverters in alternate tiers connected by TSVs is simulated using Spectre [15]. The RO is cascaded with an eight-stage frequency divider circuit at the output. R_{TSV} and C_{TSV} are varied, and their impact on the RO delay is shown in Fig. 10. Variations in R_{TSV} values for a given value of C_{TSV} do not change the RO delay significantly but RO delay increases significantly with increasing C_{TSV}. Thus, changes in R_{TSV} show minimal impact on the delay, while the impact of C_{TSV} is not negligible. The dynamic power dissipation $C_{\mathrm{TSV}} V_{\mathrm{dd}}^2 f$ is also reduced by lower TSV capacitance, and therefore, efforts should be made to reduce the TSV capacitance.

V. Summary and Conclusion

The resistance, inductance, and capacitance of a TSV are modeled as a function of physical parameters and material characteristics. Estimations of R, L, and C match very well with the numerical simulation results from Raphael and Sdevice and with experimental measurements. The impact of various technology parameters on the resistance, inductance, and capacitance of TSV has been analyzed, and the models are applied to predict the resistance, inductance, and capacitance of the small-geometry TSVs. The TSV lumped impedance model is based on these RLC elements and shows that the TSV capacitance has the most dominant impact on the delay.

Appendix

By solving (3) with the boundary conditions given in (4)–(5), the solution of the potential is derived as

$$\psi(r) = \frac{qN_a r^2}{4\varepsilon_{\mathrm{si}}} - \frac{qN_a R_{\mathrm{dep}}^2}{2\varepsilon_{\mathrm{si}}} \ln(r) + \frac{qN_a R_{\mathrm{dep}}^2}{4\varepsilon_{\mathrm{si}}} \left(2\ln(R_{\mathrm{dep}}) - 1\right). \tag{A1}$$

This solution is further elaborated to make the dependence explicit on some of the key parameters like threshold voltage and accumulation, depletion, and minimum depletion capacitance of the TSV.

A. Derivation of Threshold Voltage ($V_{\rm Th}$) of TSV

The threshold voltage of TSV is defined as the TSV voltage at which the Si$-$SiO$_2$ surface potential is equal to $2\ln(N_a/n_i)$, where n_i is the intrinsic carrier concentration of the Si substrate. This surface potential at the Si$-$SiO$_2$ interface is reached when the depletion radius is at its maximum value. Substituting $\psi|_{r=R_{\rm ox}} = 2\ln(N_a/n_i)$ and $R_{\rm dep} = R_{\rm max}$ in (A1), the maximum depletion radius is given in

$$\frac{qN_aR_{\rm ox}^2}{4\varepsilon_{\rm si}} - \frac{qN_aR_{\rm max}^2}{2\varepsilon_{\rm si}}\ln(R_{\rm ox}) + \frac{qN_aR_{\rm max}^2}{4\varepsilon_{\rm si}}\left(2\ln(R_{\rm max}) - 1\right) - 2\ln\left(\frac{N_a}{n_i}\right) = 0 \tag{A2}$$

Equation (A2) is solved iteratively to obtain the maximum depletion radius. This solution is quickly converging even for the small-geometry TSV dimensions. Total bulk charge in the radial depletion region is $Q_B = -qN_a\pi(R_{\rm max}^2 - R_{\rm ox}^2)$. The applied TSV voltage drops across the TSV oxide as well as the silicon substrate, as given in

$$V_{\rm TSV} = V_{\rm si} + V_{\rm ox}. \tag{A3}$$

By applying Gauss's law to the cylindrical MOS system and by considering the work function of the TSV metal in addition to total oxide charges ($Q_{\rm ot} = Q_f + Q_m + Q_{\rm tr}$), the expression for threshold voltage is derived as

$$V_{\rm Th} = \phi_{\rm ms} - \frac{2\pi R_{\rm ox}qQ_{\rm ot}}{2\pi\varepsilon_{\rm ox}}\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right) + 2\ln\left(\frac{N_a}{n_i}\right) + \frac{qN_a\pi\left(R_{\rm max}^2 - R_{\rm ox}^2\right)}{2\pi\varepsilon_{\rm ox}}\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right) \tag{A4}$$

where total oxide charges are composed of the fixed oxide charge (Q_f) at the Si$-$SiO$_2$ interface, mobile charges in the oxide (Q_m), and oxide trapped charges ($Q_{\rm tr}$) while $\phi_{\rm ms}$ denotes the work function difference given by $\phi_m - \phi_s$. The flatband voltage in this case equals

$$V_{\rm FB} = \phi_{\rm ms} - \frac{2\pi R_{\rm ox}qQ_{\rm ot}}{2\pi\varepsilon_{\rm ox}}\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right).$$

As in the planer case, a cylindrical TSV system has three distinct regions of operation, namely, accumulation, depletion, and inversion. The capacitance expressions in each operating region are derived in the following.

B. Accumulation Region ($V_{\rm TSV} < V_{\rm FB}$)

TSV MOSCAP is in the accumulation region when $V_{\rm TSV} < V_{\rm FB}$. The capacitance in this case is the cylindrical oxide capacitance given as

$$C_{\rm TSVACC} = C_{\rm ox} = \frac{2\pi\varepsilon_{\rm ox}l_{\rm TSV}}{\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right)}.$$

C. Depletion Region ($V_{\rm FB} \le V_{\rm TSV} < V_{\rm Th}$)

For the voltage range of $V_{\rm FB} \le V_{\rm TSV} \le V_{\rm Th}$, the substrate region is depleted of carriers and the capacitance is the series combination of $C_{\rm ox}$ and $C_{\rm dep}$ such that

$$C_{\rm TSVDEP} = \frac{C_{\rm ox}C_{\rm dep}}{C_{\rm ox} + C_{\rm dep}}.$$

The depletion capacitance is given by

$$C_{\rm dep} = \frac{2\pi\varepsilon_{\rm si}l_{\rm TSV}}{\ln\left(\frac{R_{\rm dep}}{R_{\rm ox}}\right)}$$

and $R_{\rm dep}$ is the radial depletion width obtained by solving (A5) for $R_{\rm dep}$ for a given bias $V_{\rm TSV}$.

$$V_{\rm TSV} = \phi_{\rm ms} - \frac{2\pi R_{\rm ox}qQ_{\rm ot}}{2\pi\varepsilon_{\rm ox}}\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right) + 2\ln\left(\frac{N_a}{n_i}\right) + \frac{qN_a\pi\left(R_{\rm dep}^2 - R_{\rm ox}^2\right)}{2\pi\varepsilon_{\rm ox}}\ln\left(\frac{R_{\rm ox}}{R_{\rm Metal}}\right) \tag{A5}$$

D. Minimum Depletion Capacitance Region ($V_{\rm TSV} \ge V_{\rm Th}$)

For high-frequency operation, the depletion width does not increase beyond $R_{\rm max}$, and hence, the total capacitance is the series combination of oxide capacitance and minimum depletion capacitance, providing minimal $C_{\rm TSV}$ given as

$$C_{\rm TSVMIN} = \frac{C_{\rm ox}C_{\rm dep\,min}}{C_{\rm ox} + C_{\rm dep\,min}}$$

where

$$C_{\rm dep\,min} = \frac{2\pi\varepsilon_{\rm si}l_{\rm TSV}}{\ln\left(\frac{R_{\rm max}}{R_{\rm ox}}\right)}.$$

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