INVITED PAPER

Low-Voltage Tunnel Transistors for Beyond CMOS Logic

The use of interband tunneling to obtain steep subthreshold transistors at less than 0.5 V is described in this paper; underlying theory, key parameters, and optimization of performance are discussed.

By Alan C. Seabaugh, *Fellow IEEE*, and Qin Zhang, *Member IEEE*

ABSTRACT | Steep subthreshold swing transistors based on interband tunneling are examined toward extending the performance of electronics systems. In particular, this review introduces and summarizes progress in the development of the tunnel field-effect transistors (TFETs) including its origin, current experimental and theoretical performance relative to the metal–oxide–semiconductor field-effect transistor (MOSFET), basic current-transport theory, design tradeoffs, and fundamental challenges. The promise of the TFET is in its ability to provide higher drive current than the MOSFET as supply voltages approach 0.1 V.

KEYWORDS | Subthreshold swing; tunneling; tunneling transistor

As the end of miniaturization approaches for complementary metal–oxide–semiconductor (CMOS) technology, the search for devices to extend computer performance is on. This new technology must be energy efficient, dense, and enable more device function per unit space and time. There are many device proposals, often involving new state variables and communication frameworks as discussed in recent reviews by Solomon [1], Galatsis [2], and Chen [3]. In this paper, we examine a subset of beyond CMOS technologies, those that compete directly with the MOS field-effect transistor (FET) in power, area, and speed, in a commercial temperature range 0 °C–75 °C, and in a von Neumann architecture.

These devices are aimed at supply voltages less than a 0.5 V, enabled by a lower subthreshold swing. In the metal–oxide–semiconductor field-effect transistor (MOSFET), the subthreshold swing is limited by the Boltzmann distribution of carriers to 60 mV/decade of channel current at room temperature. Switching mechanisms that can achieve less than 60 mV/decade in a FET structure include tunneling [4]–[6], impact ionization [7]–[10], ferroelectric dielectrics [11], or mechanical gates [12]–[14]. Here, we focus on the tunneling field-effect transistor (TFET) because it can be controlled at voltages well under a volt and does not have the delays associated with positive feedback that are intrinsic to impact ionization, ferroelectricity, and mechanical mechanisms.

Our treatment begins with the origins of the device [15] and the physics of operation. We then compare the demonstrated and projected TFET characteristics against current 32-nm CMOS technology to compare with the state-of-the-art. Next, we derive, repair, and add to the analytic tunneling formulas used to guide TFET design in bulk and 1-D structures. Finally, we review TFET design, scaling, and fundamental challenges.

I. INTRODUCTION

The operating principles of the TFET can be understood with the aid of the energy band diagram and device cross section of Fig. 1. This energy band diagram is computed for a graphene nanoribbon (GNR), but is a good illustration of the band profile for an ultrathin body, sub-10-nm, semiconductor transistor. With source and drain contacts and no gate, an abrupt p^+n^+ junction is shown in Fig. 1(a) with a tenth volt drain bias. Channel current flows by Zener [16] tunneling from valence band to conduction band. With a gate aligned to the p^+n^+ junction and a metal

Manuscript received August 5, 2010; accepted August 17, 2010. Date of publication October 25, 2010; date of current version November 19, 2010. This work was supported by the Nanoelectronics Research Initiative through the Midwest Institute for Nanoelectronics Discovery (MIND) and the National Institute of Standards and Technology (NIST).

A. C. Seabaugh is with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556-5637 USA (e-mail: seabaugh.1@nd.edu).

Q. Zhang was with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556-5637 USA. She is now with the Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899-8120 USA.

Digital Object Identifier: 10.1109/JPROC.2010.2070470

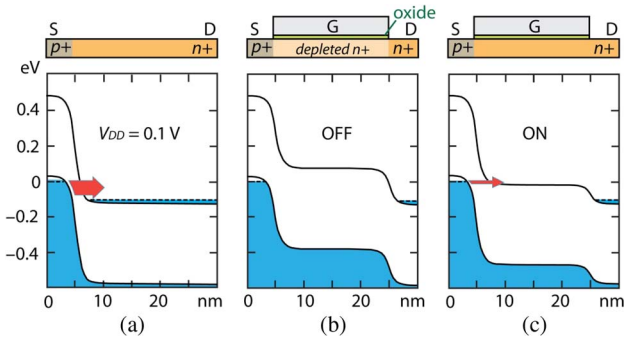

Fig. 1. *Energy band diagram and layer structure for an nTFET consisting of an n^+ source (S), p^+ drain (D), and gate (G). In (a) the Zener tunneling p^+n^+ channel is shown under 0.1-V bias without a gate. In (b), the gate fully depletes the channel at zero gate potential creating a normally off device. In (c), a positive gate voltage turns the channel on with current set by the overlap of valence band electrons with unfilled conduction band states.*

work function selected to fully deplete the channel this *n*TFET is configured for normally off, enhancement-mode operation [Fig. 1(b)]. Positive gate voltage shown in Fig. 1(c) reengages the Zener tunneling and the transistor turns on with a saturated current set by the gate-to-source voltage. The transistor is fully depleted without gate bias. In turning the transistor on, the gate bias lowers the vertical electric field normal to the gate, opposite to the case of the MOSFET where the effective mobility degrades with increasing vertical field. This embodiment of the TFET can be expected to have lower Coulomb scattering than a MOSFET or a *p*–*i*–*n* TFET.

The TFET has the basic attributes needed for a complementary logic technology in a Boolean logic architecture. The transistor has current gain, voltage gain, and input–output isolation. The current saturates with the saturation set by the source injection. Unlike the MOSFET, the *n* and *p* devices carry the same current if they use the same tunnel junction, therefore equal gate widths give equal on currents and symmetric layouts are possible. Since the Fermi tail is cutoff by the bandgap the subthreshold swing is not limited to 60 mV/decade and the OFF-current can be significantly below that of the MOSFET. As will be discussed in Sections IV and V, there are additional considerations in particular cases and geometries, which place limitations on these general statements.

The first investigation of a transistor containing the basic elements of the TFET was conducted by Stuetzer [17] in 1952, predating even Esaki's discovery of *p*–*n* interband tunneling [18]. Stuetzer showed the ambipolar nature of the current–voltage *I*–*V*, in the field gating of a lateral Ge *p*–*n* junction. He was also able to show the dependence of the transistor characteristic on gate placement with respect to the *p*–*n* junction. In 1977, Quinn *et al.* [19] proposed the formation of a surface-channel MOS tunnel junction by replacing the *n*-type source of an *n*-MOSFET with a highly degenerate *p*-type source. Their device geometry, the configuration of a lateral TFET, was intended for measurement of subband splitting and transport properties of tunneling between a bulk source and a 2-D surface channel. The first vertical TFET appears to have been proposed by Leburton *et al.* [20] with the aim of creating a high-speed transistor in which the gate was used to control the negative differential resistance (NDR).

In 1992, Baba [21] independently proposed the lateral TFET structure of Quinn for a transistor also designed to use the gate to control the NDR. This transistor was named the surface tunnel transistor (STT). The first observation of room temperature NDR in the STT was reported by Uemura and Baba in GaAs [22] in 1994. The STT was demonstrated in Si [23] in 1995 by Kawaura, and in 1996, a silicon-on-insulator (SOI) STT was demonstrated by Omura [24]. Neither of these STTs showed NDR at room temperature. In Si, room temperature NDR in the STT was demonstrated by Koga and Toriumi [25], [26]. Compound semiconductor STTs with both regrown GaAs and $In_{0.2}Ga_{0.8}As$ tunnel junctions were demonstrated by Uemura and Baba [27] in 1996, and in the following year, current densities over 1 mA/μm^2 in $In_{0.53}Ga_{0.47}As$ TFETs on InP [28] at room temperature were shown. Self-aligned regrowth processes [29] were developed in 80-nm gate-length TFETs [30] by Chun in 1999 and 2000. The focus of the STT in this period was on field control of the Esaki, forward-biased characteristic of the tunnel junction and in ways to utilize the NDR characteristic.

In 1995, Reddick and Amartunga [31] proposed gating of the reverse, Zener-tunneling current of the STT, or TFET, as a means to achieve better scaling due to the absence of "punch-through." Hansch *et al.* [32] in 2000 proposed and fabricated a Si vertical TFET to also gate the Zener side of the tunnel junction and noted its potential for low OFF-current relative to the MOSFET. In 2004, Aydin *et al.* [33] reported the characteristics of a lateral SOI embodiment of the TFET.

The first discussion of low subthreshold swing in the TFET appeared in 2004 by Wang [4], Bhuwalka [5], and Appenzeller [6], but was certainly being considered in many groups. Zhang [34] derived an analytic expression showing how the gate controls both the internal field of the tunnel junction and the band-to-band overlap, giving rise to less than 60-mV/decade swing at room temperature. Interest in TFETs has risen steadily over the past six years. At this writing, less than 60-mV/decade subthreshold swings have been reported in only a few TFETs based on carbon nanotubes (CNT) [6], [35], Si [36]–[39], Ge [40], and p^+Ge/n^+Si [41] channels.

II. TFET STATUS

Before looking deeper into the TFET it is illuminating to compare the experimental and projected state-of-the-art in TFETs against CMOS technology. For this comparison,

two figures have been prepared. The first, Fig. 2, compiles measured n- and p-channel TFET drain current per micron gate width I_D/w versus gate-to-source bias V_{GS}, for a given drain-to-source bias V_{DS}, against 32-nm node CMOS [42]. For CMOS, both high-performance (HP) and low-power (LP) technologies are shown (dashed lines); these are measured values. For the purposes of this comparison, only TFETs that exhibit less than 60 mV/decade [6], [35]–[41] or NDR in the tunnel junction in the forward current direction [43] are included. While the TFET ON-current is not dependent on gate length, the gate length is indicated in the figure as well as gate oxide thickness or equivalent oxide thickness (EOT), to provide a scale for the experimental report. The subthreshold swings demonstrated thus far are not now in a current range of interest for either HP or LP applications as the low swings typically occur at less than 1 nA/μm. Also shown for comparison are experimental results for Si impact-ionization MOSFETs (I-MOS) [8], [10] which show subthreshold swings of less than 3 mV/decade for both n- and p-channel devices. To plot these on the same scale as the TFETs and CMOS, the source voltage is fixed at 5 V for the p-channel I-MOS and −5.5 V for the n-channel transistor. These biasing requirements raise the power dissipation and restrict the use I-MOS in combinatorial logic, but clearly demonstrate steep subthreshold swing.

The demonstrated TFETs of Fig. 1 show that, with the exception of the Choi [36], the measured sub-60-mV/decade swings occur at channel currents in the pA/μm range well below a typical transistor threshold voltage. The preponderance of the reports are on Si where the fabrication approaches for self-aligning the tunnel junction to the gate are the most mature. The low tunneling currents are an inherent difficulty in Si due to the relatively high bandgap and low tunneling effective mass. Again, with the exception of the Choi findings, the use of SiGe and Ge heterojunctions improves the tunneling currents relative to the Si reports, consistent with lowering the tunnel barriers and tunneling masses in these materials. The CNT TFETs [6], [35] are in transistor geometries designed to observe

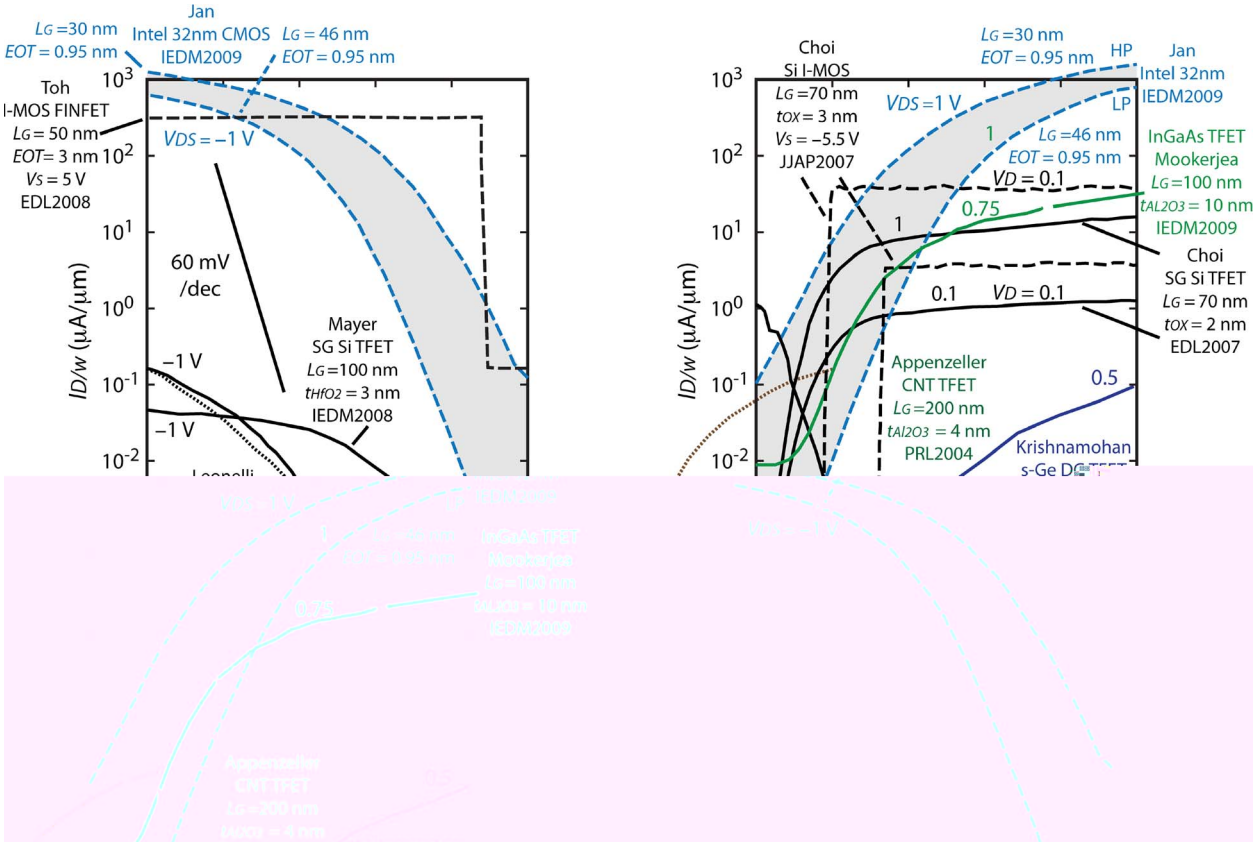

Fig. 2. ***Comparison of published TFET channel current per unit width versus gate-to-source voltage for (a) p-channel [37], [39] and (b) n-channel [6], [35], [36], [40], [41], [43] transistors. Included are devices that show a subthreshold swing less than 60 mV/decade or NDR in the forward characteristics of the tunnel junction. Dashed lines bordering the shaded area indicate measured high-performance (HP) and low-power (LP) 32-nm node MOSFET technology [42]. The black dashed lines are measured characteristics for I-MOS transistors. For I-MOS, to plot on the same scale, the source voltage is shifted and the V_{GS} indicated should be added to the listed source voltage to get the true gate-to-source voltage. The acronyms SG, DG, and MuG mean single, double, and multigate, respectively. All measurements were reported at room temperature. The CNT TFET drain current per unit width was computed by dividing the measured current by 10 nm as a representative effective tube pitch.***

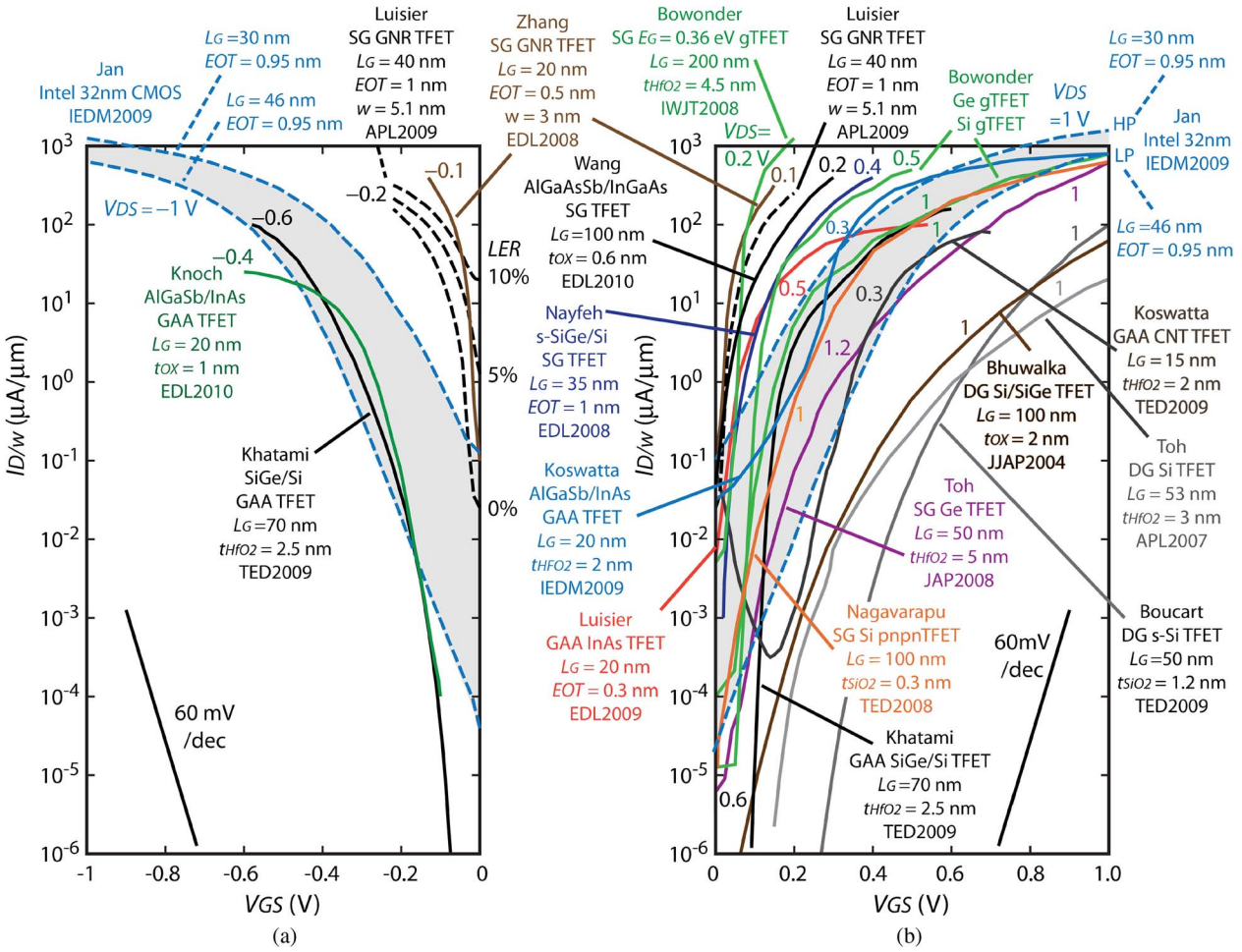

Fig. 3. ***Comparison of simulated TFET channel current per unit width versus gate-to-source voltage for (a) p-channel and (b) n-channel transistors. Light dashed lines bordering the shaded region indicate experimental high-performance (HP) and low-power (LP) 32-nm node MOSFET technology. Other notation in the figure includes SG for single gate, DG for double gate, GAA for gate-all-around, LER for line-edge roughness, and the numbers are for the drain-to-source voltages V_{DS}. The GNR currents are given per unit ribbon width.***

the low swing, using electrostatic doping to form the tunnel junctions, and not optimized for high current drive. The InGaAs TFET [43] showed NDR in the forward direction, but did not show a sub-60-mV/decade swing; this was attributed to a parasitic tunneling mechanism involving traps in the source tunnel junction.

A second figure provides the same plot of I_D/w versus V_{GS} for the theoretical TFET reports across material systems [5], [44]–[57] versus 3-nm CMOS technology. The simulations range over a wide space, but are overall consistent. Higher ON-currents at lower voltages are obtained in the lower bandgap materials like Ge [45], InAs [49] and in GNRs [44], [50]. Heterojunction systems like SiGe/Si [46], AlGaSb/InAs [52], [55], and AlGaAsSb/InGaAs [56] boost the ON-current. The wide range of TFET characteristics are clearly apparent. These variations are generally consistent with a wide design space that includes the transistor geometry (gate-all-around, double gate, or single gate), in-line or perpendicular gate orientation with respect to the tunnel junction, tunnel junction doping level and profile, and dimensionality of the transport.

For the case of GNR TFETs, Luisier and Klimeck [50] have considered how the edge roughness affects the OFF-current of the transistor. The edge roughness is parameterized by a line edge roughness (LER) probability, and the variation in the transfer characteristic with LER is indicated Fig. 3(a) by the dark dashed lines. For clarity, the *n*-channel plot [Fig. 3(b)] shows only the perfect GNR TFET from Luisier and Klimeck.

III. TFET ANALYTIC THEORY

Zener tunneling, electrons passing "from one 'energy band' into another," was first introduced by Clarence Zener in 1934 [16] to explain dielectric breakdown, a precipitous rise in current as the field strength increases.

Specifically, in a heavily doped semiconductor p^+n^+ junction, electrons in the p^+ valence band can tunnel into the n^+ conduction band under a reverse bias, an effect now called Zener tunneling and the primary transport mechanism in tunnel transistors. Zener tunneling current is determined by integrating the product of charge flux and the tunneling probability from the energy states on the p^+ side to those on the n^+ side, where the tunneling probability is calculated by applying the Wentzel–Kramers–Brillouin (WKB) approximation to the triangular potential at the p^+n^+ junction.

This section derives analytic expressions for Zener tunneling in bulk and 1-D semiconductors, which establish the principles for tunnel transistor design. In this treatment, isotropic bands are assumed for the conduction and valence bands to keep the equations simple. Nonparabolicity will raise the tunneling masses and lower the currents (transmission coefficients) relative to the parabolic band dispersion. GNR tunneling is also discussed as a special 1-D semiconductor. The current transport in GNR tunnel junctions is compared against semiconductor tunnel junctions. Finally, the definition of subthreshold swing is discussed and a practical definition is proposed.

A. Zener Tunneling

In a reverse-biased heavily doped p^+n^+ junction, shown schematically in Fig. 4(a), electrons at the valence band of the p^+ side, tunnel through the forbidden gap into the conduction band of the n^+ side. This tunneling process can be approximated by a particle penetrating a triangular potential barrier, with a height higher than its energy by the semiconductor bandgap E_G and a slope given by the electron charge times the electric field $q\xi$ [see Fig. 4(b)].

For bulk direct semiconductors, the total energy can be divided into two parts $E = E_X + E_\perp$, where $E_X = \hbar^2 k_X^2/2m_R^*$ corresponds to the energy in the tunneling direction and $E_\perp = \hbar^2(k_Y^2 + k_Z^2)/2m_R^*$ is the transverse energy which is conserved during the tunneling process, $\hbar$ is the reduced Planck constant, and the reduced effective mass $m_R^* = (1/m_E^* + 1/m_H^*)^{-1}$ averages both the electron m_E^* and hole m_H^* effective masses. The wave vector in the tunneling direction is given by

$$k_X(x) = \sqrt{\frac{2m_R^*}{\hbar^2}(E_X - U(x))} \tag{1}$$

where $U(x)$ is the potential energy profile. For a triangular tunnel barrier as shown in Fig. 4(b), the potential has the profile $U(x) = E + q\xi x$ in the region $0 < x < d$, where $d = E_G/q\xi$ and ξ is the maximum electric field at the junction [58]. The wave vector is an imaginary number when $U(x) > E_X$, and for the triangular barrier, it is given by

$$k_X(x) = \sqrt{\frac{2m_R^*}{\hbar^2}(-q\xi x - E_\perp)}. \tag{2}$$

The tunneling probability is calculated using the WKB approximation [59], $T_{\mathrm{WKB}} \approx \exp(-2\int_0^d |k_X(x)|dx)$. Therefore

$$T_{\mathrm{WKB}}^{3D} = \exp\left(-\frac{4\sqrt{2m_R^*}(E_G + E_\perp)^{3/2}}{3q\hbar\xi}\right) \cong \exp\left(-\frac{4\sqrt{2m_R^*}E_G^{3/2}}{3q\hbar\xi}\right)\exp\left(-\frac{E_\perp}{\overline{E}}\right) \tag{3}$$

where $\overline{E} = (q\hbar\xi)/(2\sqrt{2m_R^* E_G})$ is a factor, which determines the impact of the transverse-energy-state carriers on the tunneling magnitude. The larger the factor $\overline{E}$ is, the less the degradation of tunneling probability by carriers with transverse energy we have. The effect on tunneling by the transverse states is minimized by high electric field, small effective mass, and narrow bandgap.

The bulk Zener tunneling current density is calculated by integrating the product of charge flux and the tunneling probability from the Fermi energy at the p^+ side to the n^+ side [60]

$$J^{3D} = \iint q v_G(k_X)\rho_X(k_X)\rho_\perp(k_\perp)dk_X 2\pi k_\perp dk_\perp \times (f_V - f_C)T_{\mathrm{WKB}}^{3D} \tag{4}$$

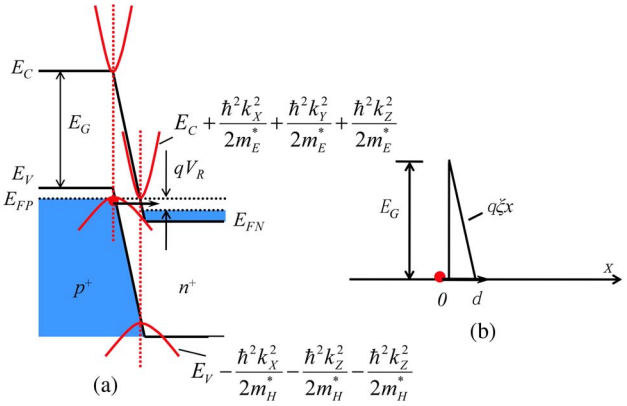

Fig. 4. *(a) Zener tunneling in a reverse-biased p^+n^+ junction for bulk semiconductors and (b) the triangular potential barrier seen by electrons tunneling in the x-direction.*

where $v_G(k_X) = (1/\hbar)dE_X/dk_X$ is the group velocity and $\rho_X(k_X) = 1\pi$ and $\rho_\perp(k_\perp) = 1/4\pi^2$ are the density of states in the tunneling direction and the transverse direction, respectively. The Fermi–Dirac distributions f_V and f_C at the valence band of the p^+ side and conduction band of the n^+ side are, respectively, $f_V(E) = [1 + \exp((E - qV_R)/qV_T)]^{-1}$ and $f_C(E) = [1 + \exp(E/qV_T)]^{-1}$, where V_R is the reverse bias, V_T is the thermal voltage, kT/q, and k is Boltzmann's constant. To simplify the calculation, $f_V - f_C \approx 1$ is assumed and then $J^{3D} \approx (qm_R^*/2\pi^2\hbar^3)\iint T_{\mathrm{WKB}}^{1D} \exp(-E_\perp/\overline{E})dE_\perp dE_X$. Integrating E_X from 0 to qV_R, $E_\perp$ from 0 to $qV_R - E_X$, and assuming $\overline{E} \ll qV_R$

$$J^{3D} = \frac{\sqrt{2m_R^*}q^3\xi V_R}{8\pi^2\hbar^2 E_G^{1/2}} \exp\left(-\frac{4\sqrt{2m_R^*}E_G^{3/2}}{3q\xi\hbar}\right). \quad (5)$$

Equation (5) is lower than Sze and Ng's equation [61] by a factor of 2 in the prefactor. This appears to be an error propagated from prior book editions, as there is no reference to an original derivation.

Although (5) is derived for direct semiconductors, it also fits well to indirect semiconductors [62]. Using (5), the dependence of tunnel current density on reverse bias is computed versus junction internal field for Si and Ge (Fig. 5). For the case of Si, measurements were taken from eight different p^+n^+ tunnel junctions [63], [64] spanning over eight orders of magnitude in current density. Equation (5) is in excellent agreement with the measurements using only the tunneling reduced effective mass as a fitting parameter and the maximum electric fields calculated from the measured doping profile. For the Ge case, the maximum electric field ξ in (5) is calculated assuming abrupt doping, because of lack of information on the doping profile, so the calculated current density is slightly higher than measurements [65]–[67]. If a 4-nm/decade dopant slope is assumed, the Ge data point [68] will shift to the calculated curve, as the electric field decreases from 2.8 to 1.6 MV/cm.

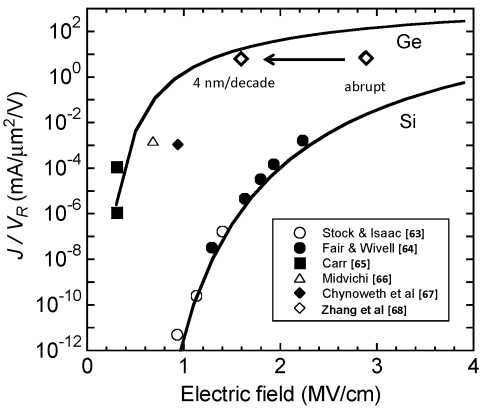

Fig. 5. *Zener tunneling current density per volt of reverse bias versus electric field for Si and Ge tunnel diodes. Close agreement is obtained between (5) and measurements with a fitted effective mass of 0.16 m_0, for Si and 0.02 m_0 for Ge.*

B. 1-D Zener Tunneling

For a 1-D direct bandgap p^+n^+ junction, the transverse energy is quantized and included in the increased bandgap. Substituting $E_\perp = 0$ in (3), the tunneling probability in a 1-D direct semiconductor is given by

$$T_{\mathrm{WKB}}^{1D} = \exp\left(-\frac{4\sqrt{2m_R^*}E_G^{3/2}}{3q\hbar\xi}\right). \quad (6)$$

Similar to bulk Zener tunneling, the 1-D Zener tunneling current is also calculated by integrating the product of charge flux and the tunneling probability from the Fermi energy level at the p^+ side to the n^+ side

$$I^{1D} = \int qv_G(k_X)\rho(k_X)(f_V - f_C)T_{\mathrm{WKB}}^{1D}\,dk_x = \frac{q^2}{\pi\hbar}T_{\mathrm{WKB}}^{1D}V_T \ln\left(\frac{1}{2}\left(1 + \cosh\frac{V_R}{V_T}\right)\right). \quad (7)$$

This derivation is given in the Appendix. If $V_R \gg V_T$, the tunneling current can be expressed as $I^{1D} = (q^2/\pi\hbar)T_{\mathrm{WKB}}^{1D}(V_R - V_T)\ln(4)$. Further, at temperature $T = 0$ K ($V_T = 0$ V), the current is proportional to the reverse bias $I^{1D} = (q^2/\pi\hbar)T_{\mathrm{WKB}}^{1D}V_R$, similar to the Landauer expression [69].

C. Zener Tunneling in GNRs

The GNR is a special 1-D semiconductor material in which the E–k relation is not parabolic but given by $E = \pm\hbar v_F\sqrt{k_X^2 + k_n^2}$ [70]. The subscript n refers to the nth subband, v_F is the Fermi velocity, equal to 10^8 cm/s [71], and k_n is the nth transverse wave vector $k_n = n\pi/3w$ [72], which is quantized by the ribbon width w, so that the bandgap is inversely related to the ribbon width $E_G = 2\hbar v_F k_1 = 2\pi\hbar v_F/3w = 1.375/w$ [73]. Here, an imaginary bandstructure calculation is used to better treat the band-to-band tunneling transport [74].

The first-subband imaginary-energy-dispersion relation of a GNR is shown in Fig. 6, computed by a tight-binding simulation. This simulation is in agreement with the analytical expression $E^{im} = \pm\sqrt{-(\hbar v_F\kappa_X)^2 + (E_G/2)^2}$, where E^{im} is the energy in the bandgap and $k_X = i\kappa_x$ is

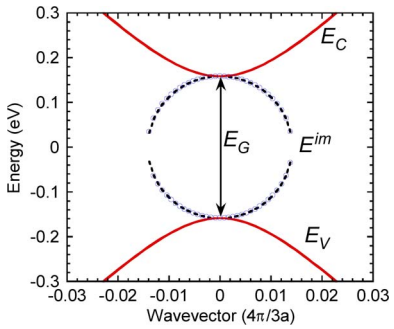

Fig. 6. *Tight-binding energy dispersion relation of the first subband of a GNR with a width of 15a, where a = 0.246 nm is the lattice constant of graphene. The solid lines are the real E–k relation and the dots are the imaginary E–k relation in the bandgap. The dashed lines show that the analytic imaginary E–k relation is in good agreement with the tight-binding simulation. This unpublished simulation is courtesy of Tian Fang, University of Notre Dame.*

the imaginary wave vector. The potential barrier seen by carriers for tunneling with energy E is

$$\frac{E_G}{2} - |E^{im}| = \frac{E_G}{2} - \sqrt{-(\hbar v_F \kappa_X)^2 + \left(\frac{E_G}{2}\right)^2} \tag{8}$$

where

$$\kappa_X = (1/\hbar v_F)\sqrt{(E_G/2)^2 - (E_C(x) - E - E_G/2)^2}$$

and

$$T_{\mathrm{WKB}}^{\mathrm{GNR}}(E) = \exp\left(-2\int \kappa_X\, dx\right) = \exp\left(-\frac{2}{\hbar v_F} \times \int_{X_I}^{X_F} \sqrt{(E_G/2)^2 - (E_C(x) - E - E_G/2)^2}\, dx\right). \tag{9}$$

Here x_I is the initial position and x_F is the final position of tunneling. Equation (9) can be used to calculate tunneling probability at all energy levels, and can be implemented in GNR TFET compact modeling.

For a reverse biased GNR p^+n^+ junction $E_C(x) - E \approx q\xi x = E_G x/d$, from Fig. 4, the tunneling probability has been derived by Jena *et al.* [75]

$$T_{\mathrm{WKB}}^{\mathrm{GNR}} = \exp\left(-\frac{2}{\hbar v_F}\int_0^d \frac{E_G}{2}\sqrt{1 - \left(\frac{2x}{d} - 1\right)^2}\, dx\right) = \exp\left(-\frac{\pi E_G^2}{4q\hbar v_F \xi}\right). \tag{10}$$

Note that the effective mass disappears in this expression due to the special E–k relation of GNRs. The Zener tunneling current has the same form as in a conventional 1-D semiconductor if only the first subband is considered [see (7)], where $T_{\mathrm{WKB}}^{1D} = T_{\mathrm{WKB}}^{\mathrm{GNR}}$.

Fig. 7 shows the room temperature tunneling current per micron ribbon width as a function of the electric field for different ribbon widths at a reverse bias of 0.1 V, using (7) and (10). With a supply voltage of 0.1 V, a tenth of the MOSFET supply voltage, GNR tunnel junctions can achieve a current density approaching 1000 μA/μm with an internal field of 4 MV/cm. At low electric field, the transmission coefficient dominates; narrower GNRs with larger bandgaps lead to lower tunneling probability and lower current density. However, the current relationship reverses at high electric fields where the $1/w$ dependence of the charge flux term becomes dominant.

For a given internal field, set by the junction, there is an optimum ribbon width that can be found by evaluating the expression $dJ/dw = d(T_{\mathrm{WKB}}^{\mathrm{GNR}}/w)/dw = 0$. Here the optimum ribbon width is $w_m = \sqrt{2\pi^3\hbar v_F/9q\xi}$ [75]. Jena [75] shows that as the electric field ξ increases from 0.5 to 5 MV/cm, the optimized ribbon width w_m monotonically decreases from 9 to 3 nm.

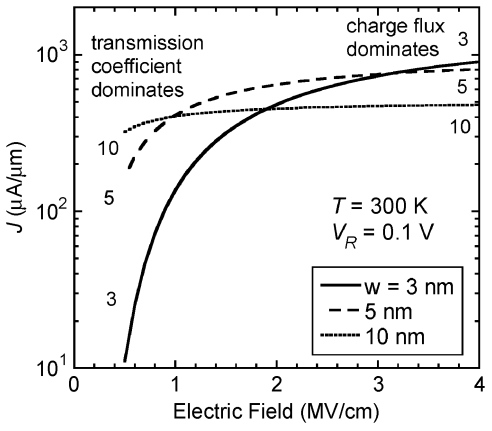

Fig. 7. *Computed room temperature Zener tunneling current density versus electric field and ribbon width in GNR p^+n^+ junctions at a reverse bias of 0.1 V.*

D. Zener Tunneling Versus Material and Dimensionality

Fig. 8 compares the tunneling current per unit width as a function of internal field for Si, Ge, InAs, InSb, and GNR lateral tunnel junctions using the material parameters in the inset table. For bulk semiconductors, a 2-nm channel thickness is assumed and quantization is neglected. The solid line, equation (5) shows that narrower band-gap materials with smaller effective mass can achieve tunneling current densities approaching that of a high-performance MOSFET. For the same electric field, Ge Zener tunneling current is more than two orders of magnitude greater than Si, while InAs and InSb are about three orders of magnitude higher. The dashed lines show the higher current per ribbon width of GNR tunnel junctions for widths of 3, 5, and 10 nm, respectively, using (7) and (10), relative to low-mass semiconductors, higher even than InSb which has a smaller bandgap. The tunneling effective masses in group IV and III-V materials depend on orientation and Fig. 8 summarizes only the [100] direction.

It is interesting to see how Zener tunneling in semiconductors junctions differs quantitatively from GNR junctions. For this comparison, the graphene ribbon width is selected to give a bandgap equal to the semiconductor bandgaps for InSb, InAs, and $In_{0.47}Ga_{0.53}As$, Fig. 9. Equation (3) is used to compute the semiconductor transmission coefficient, with $E_{\perp} = 0$, and (10) is used to determine the transmission coefficient for the GNR. For the same bandgap, the transmission coefficients for graphene and the semiconductors are nearly the same.

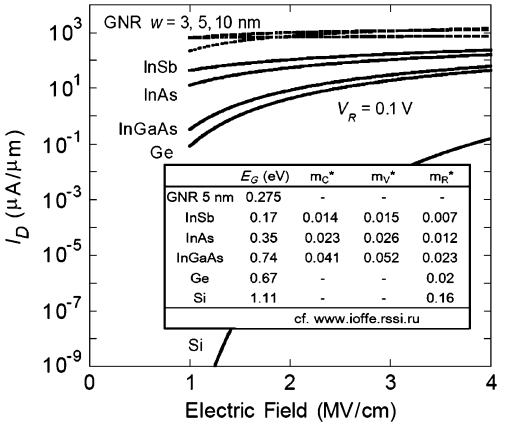

Fig. 8. *Computed Zener tunneling current density versus electric field and semiconductor material at a reverse bias of 0.1 V. The solid line shows the current per unit width for bulk semiconductors, assuming a lateral junction depth of 2 nm ignoring quantization. The dashed line shows the current per unit ribbon width of GNR tunnel junctions for widths of 3, 5, and 10 nm. The inset gives the material parameters used in (5), (7), and (10); the reduced effective masses for Ge and Si were obtained from the experimental data of Fig. 5 rather than from calculation from the bulk masses. The GNR results are the same as those plotted in Fig. 7; the widths of 3, 5, and 10 correspond to bandgaps of 0.46, 0.28, and 0.14 eV, respectively.*

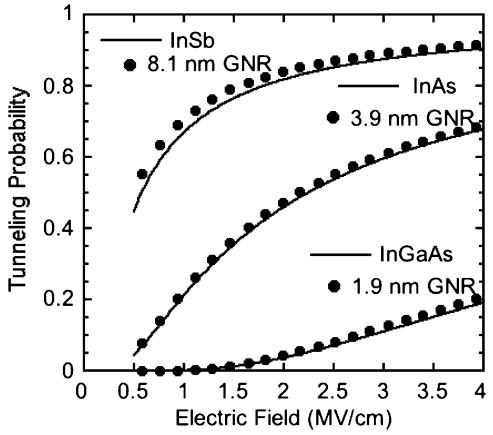

Fig. 9. *Tunneling probability versus junction electric field comparing bulk semiconductor Zener tunneling and GNR Zener tunneling with the same bandgap, using (3) and (10). The solid lines are for InSb, InAs, and $In_{0.47}Ga_{0.53}As$ tunnel junctions and the solid circles are for the GNR tunnel junction.*

This means that differences in current between GNRs and semiconductors with the same bandgap must result from differences in the source charge densities. Reconsidering Fig. 8, a higher current per unit width is predicted for graphene relative to InSb, indicating that a greater carrier density is available for tunneling in graphene.

There is a benefit in going from bulk to a 1-D tunneling transport that can be evaluated by comparing (5) and (7). Silicon and Ge are used for the comparison; the bulk transport uses a channel thickness of 2 nm while the 1-D transport uses a 2-nm NW diameter. As shown in Fig. 10,

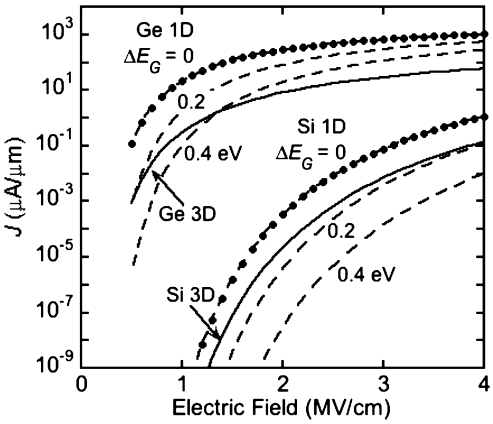

Fig. 10. *Computed Zener tunneling current density versus electric field for Si and Ge at a reverse bias of 0.1 V, using (5) and (7) at 0 K. The solid black lines show the current per unit width of a bulk semiconductor with a 2-nm channel thickness. For the 1-D case, a 2-nm diameter is used and the current per unit width is normalized by the diameter. Increases in bandgap ΔE_G, as can be expected from quantization, decrease the 1-D current.*

the 1-D tunneling gives higher Zener tunneling current per micrometer width than the bulk case. The effect of quantization can be approximated by raising the effective bandgap in the 1-D case; this increase is given in Fig. 10 by ΔE_G. As may be expected, quantization acts to reduce the 1-D Zener tunneling current density. For Ge, the 1-D tunneling current density can be higher than in bulk even with significant quantization. However, the benefit of 1-D tunneling versus bulk reduces inversely with the pitch, the center-to-center distance between NWs. For a given pitch, the effective 1-D current density in Fig. 10 must be scaled by the ratio of two over the pitch given in nanometers.

E. Subthreshold Swing

The subthreshold swing is defined by $S = (d\log I_D/dV_{GS})^{-1}$ in units of mV/decade, and in the MOSFET, it is independent of V_{GS} below the threshold voltage. For the TFET, the tunnel current can be described approximately by (5) simplified as follows:

$$I = aV_{\text{eff}}\xi \exp\left(-\frac{b}{\xi}\right) \tag{11}$$

where a and b are coefficients determined by the materials properties of the junction and the cross-sectional area of the device. Specifically, $a = Aq^3\sqrt{2m_R^*/E_G}/8\pi^2\hbar^2$ and $b = 4\sqrt{2m_R^*}E_G^{3/2}/3q\hbar$. The derivative of the tunneling current expression of (11) with respect to the gate-to-source voltage can then be used to determine an expression for the TFET subthreshold swing [76]

$$S = \ln(10)\left[\frac{1}{V_R}\frac{dV_R}{dV_{GS}} + \frac{\xi+b}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1}. \tag{12}$$

There are two terms in the denominator of (12) that should be maximized to achieve a low subthreshold swing. These terms are not explicitly limited by kT/q. According to the first term, the transistor should be engineered so that the gate-to-source voltage directly controls the tunnel junction bias or band overlap. This term suggests that the transistor geometry is optimized by a gate with strong electrostatic control, such that the gate directly changes the junction reverse bias. Assuming efficient gate electrostatics using a thin high-k gate dielectric and an ultrathin body, the gate bias directly modulates the band overlap $dV_R/dV_{GS} \approx 1$; this leaves the first term in the denominator of (12) inversely related to V_{GS}. As a consequence, the subthreshold swing decreases as gate-to-source voltage decreases. A second way that subthreshold swing is minimized is by maximizing the second term in the denominator of (12). This occurs when the gate is placed to align the applied field with the internal field of the tunnel junction. In this way, the gate field adds to the internal field to increase the tunneling probability.

Several ways to define subthreshold swing have been proposed for the TFET [77], [78]. The most often used method, as illustrated by the reports summarized in Fig. 2, is to give the tangential inverse slope of the I_D–V_{GS} curve at the steepest part of the characteristic. Bhuwalka [77] and Boucart and Ionescu [78] have proposed a definition, which will provide an average swing

$$S = \frac{V_{TH} - V_{\text{OFF}}}{\log(I_{TH}/I_{\text{OFF}})} \tag{13}$$

where V_{TH} is the threshold and V_{OFF} is the voltage below threshold at which the current I_{OFF} is a minimum. Here, the problem is to define the threshold voltage and for this the constant current method [79] can be applied. For example, as in the MOSFET, the threshold current can be defined as $I_{TH} = 10^{-7}/L_G$ ampere, where the gate length L_G is given in nanometers.

A new definition for the TFET threshold voltage, proposed by Boucart and Ionescu [80], has the threshold voltage defined as the voltage where the I_D–V_{GS} or I_D–V_{GS} characteristic transitions between quasi-exponential and linear dependence on the drain current. In this method, two threshold voltages are determined. This definition has the disadvantage that it depends strongly on the TFET junction design and gate geometry.

We propose a practical definition for effective subthreshold swing which anticipates the voltage scaling attribute of low-subthreshold-swing devices. First, define the threshold voltage to be half the supply voltage, i.e., $V_{TH} = V_{DD}/2$ and $I_{TH} = I_D(V_{GS} = V_{DD}/2)$. In this definition, the OFF-voltage equals zero, the OFF-current becomes the drain current at $V_{GS} = 0$, and the effective subthreshold swing is simply defined by $S = V_{DD}/[2\log(I_{TH}/I_{\text{OFF}})]$. Basic direct current (dc) performance of the TFET is then characterized by specifying ON-current, supply voltage, and effective S.

IV. TFET DESIGN CONSIDERATIONS

In this section, the design considerations and tradeoffs for TFETs are discussed beginning with an overview of the geometrical considerations. Also covered in this section are dependences on supply voltage, gate electrostatics, source doping, mechanisms limiting OFF-state, and progress in circuit development. Factors that can degrade swing, like interface trap density and phonon assisted tunneling near turnoff are not treated here; more experiments are needed to understand the physics of these interfaces.

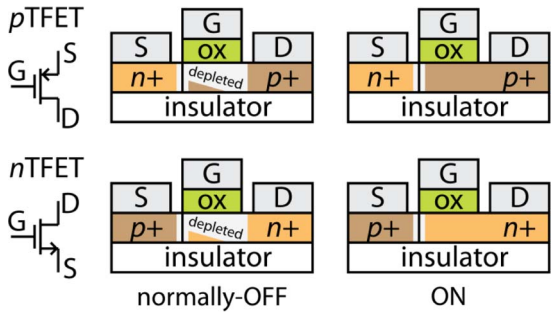

Fig. 11. *Single-gate lateral TFETs with n- and p-channels in both ON- and OFF-states.*

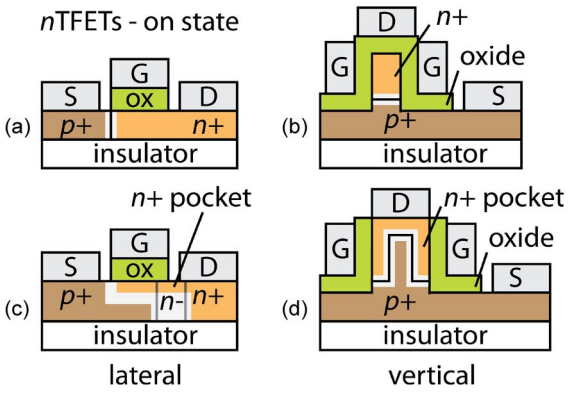

Fig. 12. *Two approaches for nTFETs. The upper row shows (a) single-gate lateral and (b) double-gate vertical structures in which the gate field originates from the surface, perpendicular to the orientation of the tunnel junction internal field. The lower row nTFETs have an n^+ pocket under the gate in a (c) lateral and (d) vertical geometry. The pocket acts to increase the area of the tunnel junction and aligns the tunnel junction internal field with the gate field to lower the subthreshold swing.*

The geometry of the TFET is illustrated in the schematic cross sections of Fig. 11. In this ultrathin-body TFET, a lateral p–n junction is formed with the gate placed on the n or p side of the junction to form either an n-channel transistor or a p-channel transistor. The metal gate work function is chosen to fully deplete the channel in the OFF-state. In the ON-state, the Zener tunneling is enabled, and to achieve high current density, abrupt doping profiles are required with degenerate doping densities. There is a tradeoff between the increased junction electric field obtained by increasing the doping degeneracy and the decrease in the band overlap as the degeneracy is increased, and this depends on the channel material. The doping must also be high enough to circumvent depletion in the access regions. This leads to channel thicknesses in the range 2–30 nm depending on the material with thicker channels possible in the narrow gap materials.

In another common TFET embodiment, the p–i–n channel profile, a MOSFET is converted into a TFET by inverting the doping type of the source; see, for example, [4]. The p–i–n TFET has a very different vertical field dependence than the device of Fig. 11. In the p–i–n TFET, the channel is an inversion layer, and like the MOSFET, the vertical field increases with gate bias. Tunneling from the source is from a bulk source into a 2-D channel. In contrast, in the fully depleted TFET of Fig. 11, the work function of the metal gate depletes the channel at zero gate bias and as the gate bias increases the vertical electric field is decreased to create a near-flatband vertical channel profile.

The gate must be self-aligned to the junction in the TFET. This is one of the key technical challenges. If the gate is underlapped, i.e., the junction is moved out from under the gate, the field control is degraded and sub-60-mV/decade swing cannot be expected. If the gate is overlapped, i.e., the junction is under the gate metal, then the field in the ON-condition is acting to deplete carriers on the source side of the junction, decreasing the tunneling injection. The gate must be placed with a high precision approaching that of the lateral potential variation length, which is typically less than 10 nm [81] in these heavily doped structures.

Like the MOSFET, gate control in the TFET is improved by moving from single-gate to double-gate geometries as illustrated in Fig. 12(a) and (b). An approach to increasing ON-current proposed by Hu [82] inserts a degenerate pocket under the gate as shown in Fig. 12(c) and (d). The pocket increases the area of the junction in the ON-state increasing the current. It also assists a lower subthreshold swing by aligning the gate field with the internal tunnel junction field. This approach lends itself to both lateral and vertical configurations. These configurations illustrate basic configurations for the TFET; more are sure to follow as processes are developed to minimize access resistance, form abrupt degenerate junctions, self-align the gate, and realize 1-D channels.

A. Supply Voltage

As gate length has scaled below 100 nm in the MOSFET, voltage has remained close to 1 V and power dissipation has become the performance limiter. Voltage scaling into the 0.5-V range is now being discussed for CMOS; see, for example, [83]. The primary benefit of the TFET is to enable higher performance at low voltages. Several groups have projected high-performance TFETs at supply voltages under 0.5 V [46], [50]–[52]. Table 1 summarized the referenced projections in bold compared with 1-V MOSFET technology. The gate capacitance C_G for the TFET is computed for a 20-nm gate length, the computed delay, and the computed power-delay product (PDP).

The low supply voltage used with the TFET is enabled by the narrow bandgap materials. Table 1 gives a few material options for TFETs with supply voltage below 0.5 V with potential for high performance with much lower power consumption than the 2009 MOSFET [84]. The

Table 1 Performance Comparison of the MOSFET at 1-V Supply With TFETs Operating Under 0.5 V. The Numbers in Bold Are Provided in the Referenced Papers. Since the TFET ON-Current Does Not Depend on Gate Length No Normalization Is Needed to Scale the ON-Current; the Gate Capacitance Used to Calculate the TFET Delay and PDP Are for a 20-nm Gate Length

Attribute	MOSFET	TFET			
V_{DD} (V)	1	0.4	0.3		0.2
L_G (nm)	29	35	15	20	40
Channel	Si [83]	Ge-Si [46]	CNT [51]	Broken gap [52]	GNR [50]
I_{ON} (μA/μm)	**1210**	**400**	**400**	**550**	**225**
C_G (fF/μm)	**0.76**	0.69	-	-	0.69
$\tau = C_G V_{DD}/I_{ON}$ (fs)	628	690	**100**	**120**	613
PDP = $C_G V_{DD}^2$ (fJ/μm)	0.76	0.11	0.012	0.020	0.028

TFET performance does not include parasitics, but is also not optimized for the supply voltage. Silicon homojunction TFETs do not appear in Table 1 because the ON-current is too low to be of interest. This can be clearly seen from the predicted TFET performances for Si shown in Fig. 3. Even with 4 GPa of stress, strained-Si double-gate TFETs have an order of magnitude lower ON-current than low-power *n*MOS at 1 V [57]; see the data of Boucart [57] in Fig. 3. Strain is still an important optimization parameter for use in the heterojunction TFET, which enables ON-current higher than *n*MOS at low voltages; see the data of Nayfeh for a strained SiGe/Si heterojunction [46] in Fig. 3.

While most of the TFET materials shown in Table 1 are new materials for CMOS integration, with the exception of strained Ge–Si [41], methods to enable transfer of all these materials onto Si are under development. For example, techniques for wafer-scale alignment of semiconducting CNTs have been demonstrated [85] and methods for integration of III-V materials on Si continue to advance [86]. With the integration of CNTs on Si it is not difficult to imagine integration of graphene for very large scale integration (VLSI) [87]. An additional fabrication challenge arises in the creation of a complementary technology using heterojunction TFETs where the *n*- and *p*-channel source-injector heterojunctions may need to be different to maximize the ON-current and ON/OFF-current ratio. Designs have been proposed for both *n* [5], [46], [52], [53], [56] and *p* [53], [55] heterojunction TFETs, but cost-efficient integration approaches need more consideration.

B. Electrostatics

While the ON-current in the TFET is insensitive to gate length, the TFET has its own short channel effects. The relevant length scale for the electrostatic potential in both MOSFETs and TFETs is described by the electrostatic length λ. The electrostatic length characterizes the distance over which the potential varies in the channel $\exp(-x/\lambda)$, where x is the position. Fig. 13 compares the computed electrostatic length [88] by solution of the Laplace equation for several FET geometries [89]. Smaller electrostatic lengths are an indicator of better electrostatic control. The improvements from SG to DG to GAA geometries are by factors of 2 and 4 for the DG and GAA relative to the SG. The electrostatic length does not vary significantly with channel material, which can be observed by comparison of the GAA Si NW simulation of Fig. 13 relative to the same calculation for InAs [81]. Fig. 13 also shows that GAA NW and GNR have smaller electrostatic lengths as may be expected from the closer proximity of the gate to the free electrons.

With the confinement of carriers to 1-D wire and GNR geometries, quantum confinement becomes important. Quantum confinement raises the effective bandgap and reduces the tunnel current. By moving to a staggered or nearly broken gap heterojunction system a good compromise can be found between strong current drive, quantum confinement, and good electrostatic control [52], [81]. The output conductance of the TFET depends sensitively on the gate electrostatics and doping; see, e.g., [68].

Thanks to the aggressive scaling of MOSFETs in recent years, high-*k* gate stack technology is advancing and has been incorporated into many of the TFETs that have exhibited sub-60-mV per decade swings; see Table 2. The

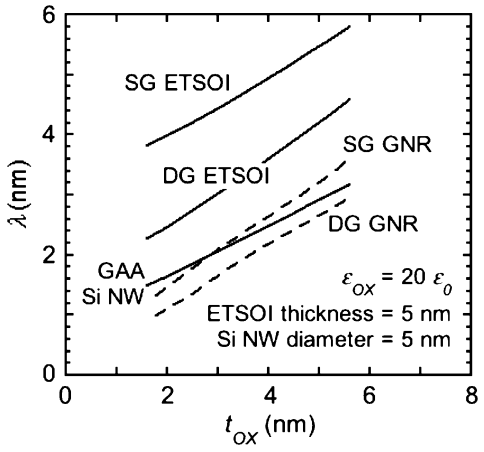

Fig. 13. *Comparison of electrostatic scaling length λ versus gate geometry in Si and GNR FETs. Acronyms: single-gate (SG), double-gate (DG), extremely thin silicon-on-insulator (ETSOI), gate-all-around (GAA), nanowire (NW), and GNR.*

Table 2 Gate Parameters for Experimentally Demonstrated TFETs With Subthreshold Swing Less Than 60 mV/decade

Author	Ref.	Structure	L_G (nm)	Gate dielectric	EOT (nm)	S (mV/dec)
Appenzeller	6	SG CNT	200	4 nm Al_2O_3	2	40
Lu	35	SG CNT	75	2 nm HfO_2	0.3	50
Mayer	37	SG Si	100	3 nm HfO_2	0.5	42
Jeon	38	SG Si	20000	HfO_2	0.9	46
Leonelli	39	MuG Si	160	2 nm HfO_2	1.3	46
Krishnamohan	40	DG Ge	1000	35 nm SiO_2	35	50
Kim	41	SG Ge/Si	5000	3 nm SiO_2	3	40

equivalent oxide thicknesses (EOT) for the TFETs utilizing high-k dielectrics are below 2 nm. Thus far, low subthreshold swings are not demonstrated on any III-V channel TFET. Experiments by Mookerjea *et al.* [90] on vertical InGaAs TFETs indicate that interface traps at the high-k Al_2O_3/InGaAs are responsible for the degradation in subthreshold swing.

C. Source Doping

The source-to-channel doping must be heavy and abrupt to maximize ON-current in the TFET. Dopant abruptness less than 4 nm/decade is needed to maximize the junction electric fields and enable high ON-currents. There are tradeoffs, however, as source doping is raised. Shown in Fig. 14(a) is a schematic energy band diagram of the source-to-channel junction of an nTFET with a degenerate p^+ source in the ON-condition. The degeneracy reduces the number of electrons available for tunneling, reducing the ON-current and degrading the subthreshold swing [52], [55]. Because of the temperature dependence of the Fermi tail [Fig. 14(b)], the degeneracy also introduces an unnecessarily strong temperature dependence to the ON-current. The heavy doping and low gate-to-drain bias in the TFET also leads to a higher gate-to-drain Miller capacitance than in the MOSFET [91].

Since the most compelling property of the TFET is the sub-60-mV/decade subthreshold swing, the source doping should be chosen to place the Fermi level in line with the source majority carrier band edge or slightly into the band [52]. In lieu of higher source dopings, the ON-current can be further increased through the use of staggered [55], [56] or broken-gap heterojunction [52] and pockets [45].

D. OFF-State

There are five primary leakage mechanisms contributing to the OFF-state current in the TFET. The first two are well known: gate leakage through the high-k gate stack and thermionic emission over the source-drain built-in potential. In addition, Shockley–Read–Hall generation in the heavily doped source and drain depletion regions is illustrated in Fig. 15(a). As gate lengths approach 20 nm, direct tunneling as well as defect-assisted tunneling become dominant especially for the narrow bandgap channels like InAs [49] and for GNRs [50]. With good gate control, even for narrow gap materials like InAs with a 20-nm gate length, direct tunneling currents can be expected to be less than 10 pA/μm [49].

A condition to be avoided is illustrated Fig. 15(c). If power supply voltage exceeds E_G/q, reverse tunneling at the drain can inject minority carriers into the channel

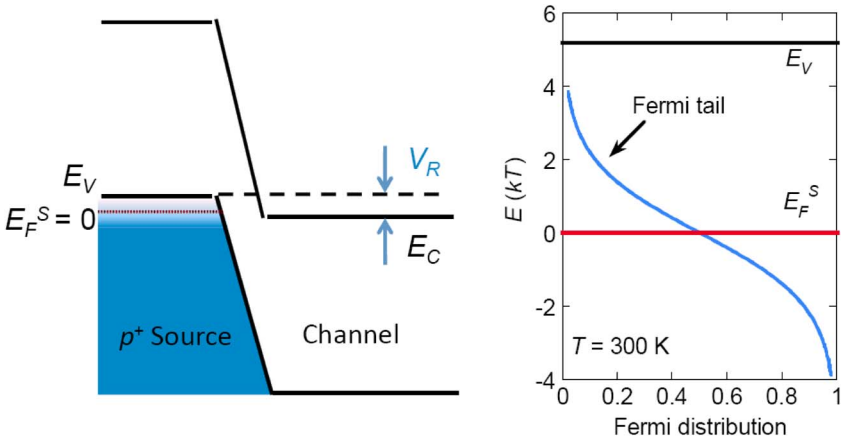

Fig. 14. *(a) Schematic energy band diagram of the source-to-channel junction of an nTFET with a degenerated p^+ source and (b) the Fermi distribution of the source at room temperature.*

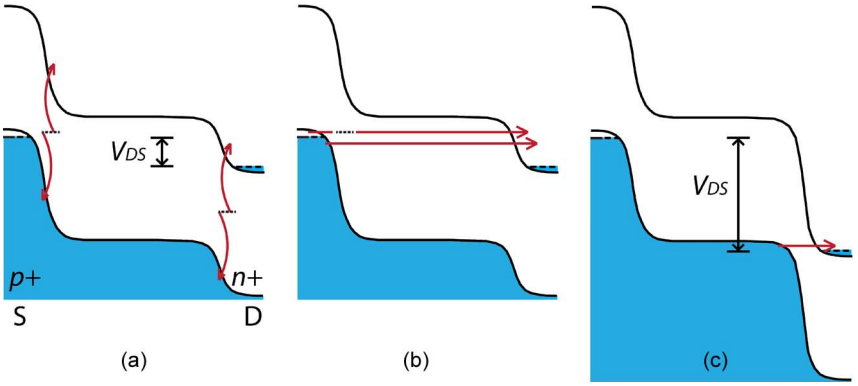

Fig. 15. *Energy band diagrams showing nTFET leakage mechanisms in the OFF-state: (a) Shockley–Read–Hall generation in the source (S) and drain (D) regions; (b) direct and defect-assisted tunneling from source to drain; and (c) hole injection at the drain.*

(ambipolar conduction). If a higher supply voltage is required to obtain ON-current, the minority carrier injection can be suppressed by building in asymmetry into the drain. One way is to use an underlapped drain or lower the doping on the drain side to make the channel-drain tunnel junction width larger than the source-channel junction [40], [47], [92]. The other way is to introduce a heterojunction, using small bandgap material in the source and larger bandgap material in the channel and the drain [40]. These two solutions can be combined.

E. Circuit Status

It is early to provide a compelling estimate of the circuit performance of TFETs. Currently, there are projections based on circuit models generated from a variety of TFET simulations [53], [93]–[95] as seen in Fig. 3. The most recent of these projections is contained in this special issue [96] showing that the greatest promise for the TFET is in low-voltage, low-power applications. At this stage, the greatest value of these assessments is in setting the application focus and discovering potential device issues, e.g., the higher Miller capacitance, 2× relative to the MOSFET [91] or new ways to construct SRAM [95].

V. CONCLUSION

A review of the TFET shows a device with potential to significantly lower subthreshold swing thereby lowering supply voltage and power dissipation. High ON-currents, exceeding 100 μA/μm, are predicted using narrow bandgap materials and staggered-bandgap heterojunctions. Theory, models, and projections are in need of experimental verification to understand the properties and evaluate the potential of tunnel transistors. The key technical challenges are in the development of advanced processes for nanoscale III-V transistors: gate alignment, low-interface-trap-density gate stacks, accurate and abrupt tunnel junctions, and low-resistance contacts. ■

APPENDIX
1-D ZENER TUNNELING

The steps leading to (7) in direct semiconductors are provided as follows:

$$
\begin{aligned}
I^{1D} &= \int q v_g(k_X)\rho(k_X)(f_V - f_C)T^{1D}_{\mathrm{WKB}}\,dk_X \\
&= \int q\frac{1}{\hbar}\frac{dE}{dk_X}\frac{1}{\pi}\left(\frac{1}{1+\exp((E-qV_R)/qV_T)}\right. \\
&\qquad \left. -\frac{1}{1+\exp(E/qV_T)}\right)T^{1D}_{\mathrm{WKB}}\,dk_X \\
&= \frac{q}{\pi\hbar}T^{1D}_{\mathrm{WKB}}\int dE\left[\left(1-\frac{\exp((E-qV_R)/qV_T)}{1+\exp((E-qV_R)/qV_T)}\right)\right. \\
&\qquad \left. -\left(1-\frac{\exp(E/qV_T)}{1+\exp(E/qV_T)}\right)\right] \\
&= \frac{q}{\pi\hbar}T^{1D}_{\mathrm{WKB}}qV_T[-\ln(1+\exp((E-qV_R)/qV_T)) \\
&\qquad +\ln(1+\exp(E/qV_T))]_{E=0}^{qV_R} \\
&= \frac{q^2}{\pi\hbar}T^{1D}_{\mathrm{WKB}}V_T[-\ln 2+\ln(1+\exp(-V_R/V_T)) \\
&\qquad +\ln(1+\exp(V_R/V_T))-\ln 2] \\
&= \frac{q^2}{\pi\hbar}T^{1D}_{\mathrm{WKB}}V_T \\
&\quad \times\ln\left[\frac{(1+\exp(-V_R/V_T))(1+\exp(V_R/V_T))}{4}\right] \\
&= \frac{q^2}{\pi\hbar}T^{1D}_{\mathrm{WKB}}V_T\ln\left[\frac{2+\exp(-V_R/V_T)+\exp(V_R/V_T)}{4}\right] \\
&= \frac{q^2}{\pi\hbar}T^{1D}_{\mathrm{WKB}}V_T\ln\left[\frac{1}{2}\left(1+\cosh\frac{V_R}{V_T}\right)\right]
\end{aligned}
$$

Acknowledgment

The authors would like to thank many people for useful discussions: T. Fang, P. Fay, T. Kosel, Y. Lu, D. Jena, T. Vasen, H. G. Xing, D. Wheeler, and G. Zhou (University of Notre Dame); S. Koswatta and J. Welser (IBM); S. Datta and T. Mayer (Pennsylvania State University); and G. Klimeck and M. Luisier (Purdue University).

REFERENCES

[1] P. M. Solomon, *Device Proposals for Beyond Silicon CMOS*, IBM Res. Rep. RC24963, Mar. 2010, pp. 1–13. [Online]. Available: http://domino.watson.ibm.com/library/CyberDig.nsf/home

[2] K. Galatsis, A. Khitun, R. Ostroumov, K. L. Wang, W. R. Dichtel, E. Plummer, J. F. Stoddart, J. I. Zink, J. Y. Lee, Y.-H. Xie, and K. W. Kim, "Alternative state variables for emerging nanoelectronic devices," *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 66–75, Jan. 2009.

[3] A. Chen, A. P. Jacob, C. Y. Sung, K. L. Wang, A. Khitun, and W. Porod, "Collective-effect state variables for post-CMOS logic applications," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2009, pp. 132–133.

[4] P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weiss, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power application," *Solid-State Electron.*, vol. 48, no. 12, pp. 2281–2286, 2004.

[5] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp^+ layer," *Jpn. J. Appl. Phys.*, vol. 43, pp. 4073–4078, 2004.

[6] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, pp. 196805-1–196805-4, Nov. 2004.

[7] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in *Proc. Int. Electron Devices Meeting*, 2002, pp. 289–292.

[8] W. Y. Choi, J. D. Lee, and B.-G. Park, "Integration process of impact ionization metal-oxide-semiconductor devices with tunneling field-effect transistors and metal-oxide-semiconductor field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 46, no. 1, pp. 122–124, 2007.

[9] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, "Low subthreshold slope in junctionless multigate transistors," *Appl. Phys. Lett.*, vol. 96, 102106, Mar. 2010.

[10] E.-H. Toh, G. H. Wang, L. Chan, D. Weeks, M. Bauer, J. Spear, S. G. Thomas, G. Samudra, and Y.-C. Yeo, "Cointegration of in situ doped silicon-carbide source and silicon-carbon i-region in p-channel silicon nanowire impact-ionization transistor," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 731–733, Jul. 2008.

[11] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.

[12] H. Nathanson, W. Newell, R. Wickstro, and J. Davis, "Resonant gate transistor," *IEEE Trans. Electron Devices*, vol. ED-14, no. 3, pp. 117–133, Mar. 1967.

[13] A. M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M. J. Declercq, P. Renaud, C. Hilbert, P. Fluckiger, and G. A. Racine, "Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal-over-gate architecture," in *Proc. Int. Symp. Quality Elecron. Design*, 2002, pp. 496–501.

[14] H. Kam, D. T. Lee, R. T. Howe, and T.-J. King, "A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics," in *Proc. Int. Electron Devices Meeting*, 2005, pp. 463–466.

[15] A. M. Ionescu, K. Boucart, K. E. Moselund, V. Pott, and D. Tsamados, "Small slope micro/nano-electronic switches," in *Proc. Int. Semicond. Conf.*, 2007, pp. 397–402.

[16] C. Zener, "A theory of electrical breakdown of solid dielectrics," *Proc. R. Soc.*, vol. A145, pp. 523–529, 1934.

[17] O. M. Stuetzer, "Junction fieldistors," *Proc. IRE*, vol. 40, no. 11, pp. 1377–1381, Nov. 1952.

[18] L. Esaki, "New phenomenon in narrow germanium p-n junctions," *Phys. Rev.*, vol. 109, no. 2, pp. 603–604, 1958.

[19] J. Quinn, G. Kawamoto, and B. McCombe, "Subband spectroscopy by surface channel tunneling," *Surface Sci.*, vol. 73, no. 1, pp. 190–196, 1978.

[20] J. P. Leburton, J. Kolodzey, and S. Biggs, "Bipolar tunneling field-effect transistor: A three-terminal negative differential resistance device for high-speed applications," *Appl. Phys. Lett.*, vol. 52, no. 9, pp. 1608–1620, May 1988.

[21] T. Baba, "Proposal for surface tunnel transistors," *Jpn. J. Appl. Phys.*, vol. 31, no. 4B, pp. L455–L457, 1992.

[22] T. Uemura and T. Baba, "First observation of negative differential resistance in surface tunnel transistors," *Jpn. J. Appl. Phys.*, vol. 33, pp. L207–L210, 1994.

[23] H. Kawaura, N. Iguchi, and T. Baba, "Fabrication of silicon surface tunnel transistors," *Ext. Abstr. Quantum Funct. Devices*, p. 62, 1995.

[24] Y. Omura, "Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors)," *Jpn. J. Appl. Phys.*, vol. 35, no. 11A, pp. L1401–L1403, 1996.

[25] J. Koga and A. Toriumi, "Negative differential conductance at room temperature in three-terminal silicon surface junction tunnel transistor," *Appl. Phys. Lett.*, vol. 70, no. 16, pp. 2138–2140, Feb. 1997.

[26] J. Koga and A. Toriumi, "Three-terminal silicon surface junction tunnel device for room temperature operation," *IEEE Electron Device Lett.*, vol. 20, no. 10, pp. 529–531, Oct. 1999.

[27] T. Uemura and T. Baba, "First demonstration of a planar-type surface tunnel transistor (STT): Lateral interband tunnel device," *Solid-State Electron.*, vol. 40, pp. 519–522, 1996.

[28] T. Uemura and T. Baba, "Large enhancement of interband tunneling current densities of over 10^5 A/cm^2 in $In_{0.53}Ga_{0.47}As$-based surface tunnel transistors," *IEEE Electron Dev. Lett.*, vol. 18, no. 5, pp. 225–227, 1997.

[29] Y. J. Chun, T. Uemura, and T. Baba, "Self-aligned surface tunnel transistors fabricated by a regrowth technique," *Jpn. J. Appl. Phys.*, vol. 38, no. 10B, pt. 2, pp. L1163–L1165, Oct. 1999.

[30] Y. J. Chun, T. Uemura, and T. Baba, "Fabrication of self-aligned surface tunnel transistors with a 80-nm gate length," *Jpn. J. Appl. Phys.*, vol. 39, no. 12B, pt. 2, pp. L1273–L1276, Dec. 2000.

[31] W. M. Reddick and G. A. J. Amartunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494–496, Jul. 1995.

[32] W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films*, vol. 369, pp. 387–389, 2000.

[33] C. Aydin, A. Zaslevsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Appl. Phys. Lett.*, vol. 84, no. 10, pp. 1780–1782, Mar. 2004.

[34] Q. Zhang, W. Zhao, and A. Seabaugh, "Analytic expression and approach for low subthreshold-swing tunnel transistors," in *Device Res. Conf. Dig.*, pp. 161–162.

[35] Y. Lu, S. Bangsaruntip, X. Wang, L. Zhang, Y. Nishi, and H. Dai, "DNA functionalization of carbon nanotubes for ultrathin atomic layer deposition of high k dielectrics for nanotube transistors with 60 mV/decade switching," *J. Amer. Chem. Soc.*, vol. 128, no. 11, pp. 3518–3519, 2006.

[36] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, pp. 743–745, Aug. 2007.

[37] F. Mayer, C. L. Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible tunnel FET performance," in *Proc. Int. Electron Devices Meeting*, 2008, pp. 163–166.

[38] K. Jeon, W.-Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J. K. Liu, and C. Hu, "Si tunnel transistors with a novel silicided source and 46 mV/dec swing," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2010, pp. 121–122.

[39] D. Leonelli, A. Vandooren, R. Rooyackers, A. S. Verhulst, S. D. Gendt, M. M. Heyns, and G. Groeseneken, "Performance enhancement in multi gate tunneling field effect transistors by scaling the fin-width," *Jpn. J. Appl. Phys.*, vol. 49, 04DC10, 2010.

[40] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and < 60 mV/dec subthreshold slope," in *Proc. Int. Electron Devices Meeting*, pp. 947–949.

[41] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2009, pp. 178–179.

[42] C.-H. Jan, "A 32 nm SoC platform technology with 2nd generation high-k metal gate transistors optimized for ultra low power,

high performance, and high density product applications," in *Proc. Int. Electron Devices Meeting*, 2009, pp. 281.1–281.4.

[43] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu, and S. Datta, "Experimental demonstration of 100 nm channel length $In_{0.53}Ga_{0.47}As$-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in *Proc. Int. Electron Devices Meeting*, 2009, pp. 137.1–137.4.

[44] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.

[45] A. Bowonder, P. Patel, K. Jeon, J. Oh, P. Majhi, H.-H. Tseng, and C. Hu, "Low-voltage green transistor using ultra shallow junction and hetero-tunneling," in *Proc. Int. Workshop Junction Technol.*, 2009, pp. 93–96.

[46] O. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis, "Design of tunneling field-effect transistors using strained-silicon/strained germanium type-II staggered heterojunctions," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1074–1077, Sep. 2008.

[47] E.-H. Toh, G. H. Wang, G. Samudra, and Y.-C. Yeo, "Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications," *J. Appl. Phys.*, vol. 103, pp. 1–5, 2008, 104504.

[48] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (pnpn) n-MOSFET: A novel high performance transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.

[49] M. Luisier and G. Klimeck, "Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 602–604, Jun. 2009.

[50] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.*, vol. 94, 223505, 2009.

[51] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456–465, Mar. 2009.

[52] S. Koswatta, S. Koester, and W. Haensch, "1D broken-gap tunnel transistor with MOSFET-like on-currents and sub-60 mV/dec subthreshold swing," in *Proc. Int. Electron Devices Meeting*, pp. 375.1–375.4.

[53] Y. Khatami and K. Banerjee, "Steep subthreshold slope n- and p-type tunnel-FET devices for low-power and energy-efficient digital circuits," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2752–2761, Nov. 2009.

[54] E.-H. Toh, G. H. Wang, G. Samudra, and Y.-C. Yeo, "Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization," *Appl. Phys. Lett.*, vol. 90, pp. 1–3, 2007, 263507.

[55] J. Knoch and J. Appenzeller, "Modeling of high-performance p-type III-V heterojunction tunnel FETs," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 305–307, Apr. 2010.

[56] L. Wang, E. Yu, Y. Taur, and P. Asbeck, "Design of tunneling field-effect transistors based on staggered heterojunctions for ultralow-power applications," *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 431–433, Apr. 2010.

[57] K. Boucart, W. Riess, and A. M. Ionescu, "Lateral strain profile as key technology booster for all-silicon tunnel FETs," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 656–658, Jun. 2009.

[58] G. A. M. Hurkx, "On the modeling of tunneling currents in reversed-biased *p–n* junctions," *Solid-State Electron.*, vol. 32, no. 8, pp. 665–668, 1989.

[59] L. D. Landau and E. M. Lifshitz, *Quantum Mechanics*. Reading, MA: Addison-Wesley, 1958, p. 174.

[60] J. L. Moll, *Physical and Quantum Electronics*. New York: McGraw-Hill, 1964, pp. 249–253.

[61] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 2007, p. 103.

[62] M. I. Nathan, "Current voltage characteristics of germanium tunnel diodes," *J. Appl. Phys.*, vol. 33, no. 4, pp. 1460–1469, 1962.

[63] J. M. Stork and R. D. Isaac, "Tunneling in base-emitter junctions," *IEEE Trans. Electron Devices*, vol. ED-30, no. 11, pp. 1527–1534, Nov. 1983.

[64] R. B. Fair and H. W. Wivell, "Zener and avalanche breakdown in As-implanted low-voltage Si n-p junctions," *IEEE Trans. Electron Devices*, vol. ED-23, no. 5, pp. 512–518, May 1976.

[65] W. N. Carr, "Energy band parameters of germanium indicated by tunnel diode reverse characteristics," *J. Appl. Phys.*, vol. 34, no. 8, pp. 2467–2472, 1963.

[66] I. Midvichi, "Study of the reverse characteristics of tunnel diodes prepared from Sb doped Ge, in the region of indirect tunnel current," *Phys. Stat. Sol*, vol. 7, pp. K95–K99, 1964.

[67] A. G. Chynoweth, W. L. Feldmann, C. A. Lee, R. A. Logan, and G. L. Pearson, "Internal field emission at narrow silicon and germanium p-n junctions," *Phys. Rev.*, vol. 118, no. 2, pp. 425–434, 1960.

[68] Q. Zhang, S. Sutar, T. Kosel, and A. Seabaugh, "Fully-depleted Ge interband tunnel transistor: Modeling and junction formation," *Solid-State Electron.*, vol. 53, no. 1, pp. 30–35, 2009.

[69] R. Landauer, "Spatial variation of currents and fields due to localized scatterers in metallic conduction," *IBM J. Res. Develop.*, vol. 1, no. 3, pp. 223–231, 1957.

[70] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Appl. Phys. Lett.*, vol. 91, 092109, 2007.

[71] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," *Science*, vol. 312, no. 5777, pp. 1191–1196, 2006.

[72] L. Brey and H. A. Fertig, "Electronic states of graphene nanoribbons studied with the Dirac equation," *Phys. Rev. B*, vol. 73, no. 23, 235411, Jun. 2006.

[73] B. Trauzettel, D. V. Bulaev, D. Loss, and G. Burkard, "Spin qubits in graphene quantum dots," *Nature Phys.*, vol. 3, pp. 192–196, 2007.

[74] T. S. Xia, L. F. Register, and S. K. Banerjee, "Calculations and applications of the complex band structure for carbon nanotube field-effect transistors," *Phys. Rev. B*, vol. 70, 045322, 2004.

[75] D. Jena, T. Fang, Q. Zhang, and H. Xing, "Zener tunneling in semiconductor nanotube and graphene nanoribbon p-n junctions," *Appl. Phys. Lett.*, vol. 93, 112106, 2008.

[76] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297–300, Apr. 2006.

[77] K. Bhuwalka, J. Schulze, and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1541–1547, Jul. 2005.

[78] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-k gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[79] A. Oritiz-Conde, F. J. G. Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Reliab.*, vol. 42, pp. 583–596, 2002.

[80] K. Boucart and A. M. Ionescu, "A new definition of threshold voltage in tunnel FETs," *Solid-State Electron.*, vol. 52, no. 9, pp. 1318–1323, 2008.

[81] Y. Lu, A. Seabaugh, P. Fay, S. J. Koester, S. E. Laux, W. Haensch, and S. O. Koswatta, "Geometry dependent tunnel FET performance—Dilemma of electrostatics vs. quantum confinement," in *Proc. Device Res. Conf.*, 2010, pp. 17–18.

[82] C. Hu, "Green transistor as a solution to the IC power crisis," in *Proc. Int. Conf. Solid-State Integr.-Circuit Technol.*, 2008, pp. 16–20.

[83] L. Chang, D. J. Frank, R. K. Montoye, S. J. Koester, B. L. Ji, P. W. Coteus, R. H. Dennard, and W. Haensch, "Practical strategies for power-efficient computing technologies," *Proc. IEEE*, vol. 98, no. 2, pp. 215–236, Feb. 2010.

[84] International Technology Roadmap for Semiconductors, *Process Integration, Devices, and Structures*, 2009 Ed., Table PIDS2, accessed Jul. 2010. [Online]. Available: www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_PIDS.pdf

[85] H. Wei, N. Patil, J. Zhang, A. Lin, H.-Y. Chen, H.-S. Wong, and S. Mitra, "Efficient metallic carbon nanotube removal readily scalable to wafer-level VLSI CNFET circuits," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2010, pp. 237–238.

[86] M. Yokoyama, Y. Urabe, T. Yasuda, H. Takagi, H. Ishii, N. Miyata, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "High mobility III-V-on-insulator MOSFETs on Si with ALD- Al_2O_3 BOX layers," in *Proc. Very Large Scale Integr. (VLSI) Technol. Symp.*, 2010, pp. 235–236.

[87] Y. Awano, "Graphene for VLSI: FET and interconnect applications," in *Proc. Int. Electron Devices Meeting*, 2009, pp. 233–236.

[88] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, Sep. 2000.

[89] Q. Zhang, Y. Lu, G. H. Xing, C. A. Richter, S. J. Koester, and S. O. Koswatta, "Graphene nanoribbon Schottky-barrier FETs for end-of-the-roadmap CMOS: Challenges and opportunities," in *Proc. Device Res. Conf.*, 2010, pp. 75–76.

[90] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent-characteristics of a vertical tunnel FET," *IEEE Electron*

Device Lett., vol. 31, no. 6, pp. 564–566, Jun. 2010.

[91] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, "On enhanced Miller capacitance effect in interband tunnel transistors," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1102–1104, Oct. 2009.

[92] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon," *Nano Lett.*, vol. 9, no. 2, pp. 684–688, 2009.

[93] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, "Effective capacitance and drive current for tunnel FET (TFET) CV/I estimation," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2092–2098, Sep. 2009.

[94] N. N. Mojumder and K. Roy, "Band-to-band tunneling ballistic nanowire FET: Circuit-compatible device modeling and design of ultra-low-power digital circuits and memories," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2193–2201, Oct. 2009.

[95] J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta, N. Vijaykrishnan, and D. Pradhan, "A novel Si-tunnel FET based SRAM design for ultra low-power 0.3 V VDD applications," in *Proc. Design Autom. Conf.*, 2010, pp. 181–186.

[96] K. Bernstein, R. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and architecture outlook for beyond CMOS switches *Proc. IEEE*, vol. 98, no. 12, Dec. 2010, DOI: 10.1109/JPROC.2010.2066530.

ABOUT THE AUTHORS

Alan C. Seabaugh (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, in 1985.

He joined the University of Notre Dame, Notre Dame, IN, in August 1999, as a Professor of Electrical Engineering following positions at the National Bureau of Standards (1979–1986), Texas Instruments Incorporated (1986–1997), and Raytheon Systems Company (1997–1999). He has authored/coauthored more than 200 papers, holds 22 U.S. patents, and has over 80 invited presentations. He is the Director of the SRC-NRI Midwest Institute for Nanoelectronics Discovery (MIND), and Associate Director of the Notre Dame Center for Nano Science and Technology. His current research interests include application of tunneling phenomena in nanoelectronics, low-power, high-performance transistors, circuits, and memory, and energy conversion devices.

Qin Zhang (Member, IEEE) received the B.S. degree in electronic engineering from Tsinghua University, Beijing, China, in 2003 and the M.S. and Ph.D. degrees in electrical engineering from the University of Notre Dame, Notre Dame, IN, in 2005 and 2009, respectively.

As recipient of the National Institute of Standards and Technology (NIST)/Midwest Institute for Nanoelectronics Discovery (MIND) Postdoctoral Fellowship, she currently works at the NIST's Semiconductor Electronics Division, Gaithersburg, MD. Her research interests include tunneling devices and graphene electronics.