Session 3: Solid State Devices

Silicon on Insulator

Outline

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- A
  - B
  - C
  - D
  - E
- F
  - G
- H
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- Ref: Taur and Ning

SOI Technology

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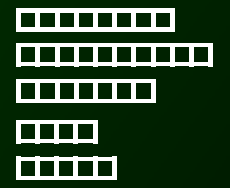


SOI materials: SIMOX, BESOI, and Smart Cut

SIMOX : Synthesis by IMplanted OXygen.

☺ thickness uniformity of the thin SOI layer

☹ high defect densities in Si and SiO2

BESOI : Bond and Etch back

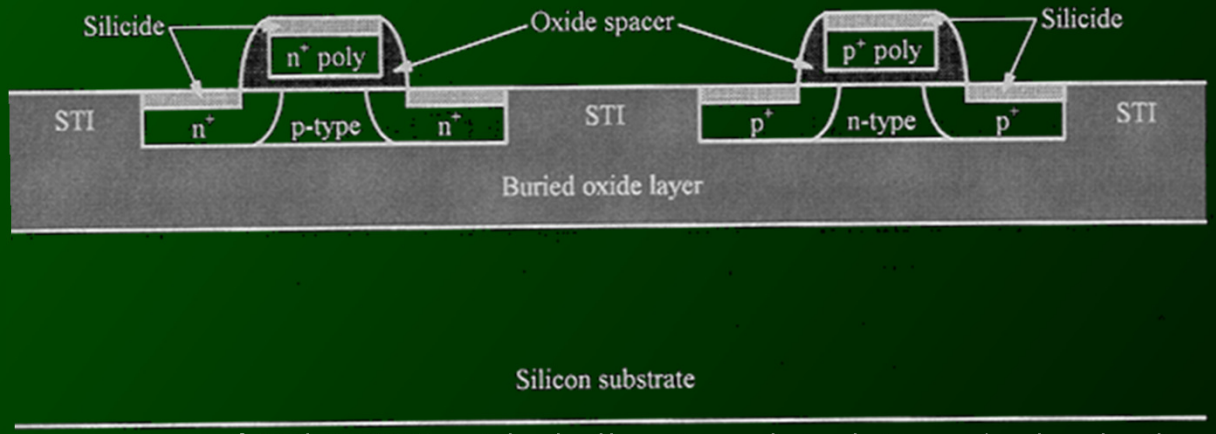
☺ Good crystalline quality

☹ thickness variation

Smart Cut: both ion implantation and bonding are used

H2 implantation

SOI CMOS



schematic cross-section of SOI CMOS, with shallow trench isolation, dual polysilicon gates, and self-aligned silicide.

- ☺ Very low junction capacitance
- ☺ No body effect
- ☺ No latch-up
- ☺ Ease in scaling
- ☺ Simpler device isolation (denser)
- ☺ Compatible with conv. Si processing
- ☺ (Sometimes) fewer steps to fabricate
- ☺ Reduced leakage
- ☺ Soft error immunity

- ☹ Drain Current Overshoot
- ☹ kink effect
- ☹ floating body (History-dependent)
- ☹ Thickness control (fully depleted operation)
- ☹ Surface states

Partially Depleted SOI MOSFETs

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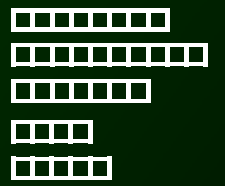


partially depleted (PD) : silicon film is thicker than the maximum gate depletion width and the devices exhibit floating-body effect

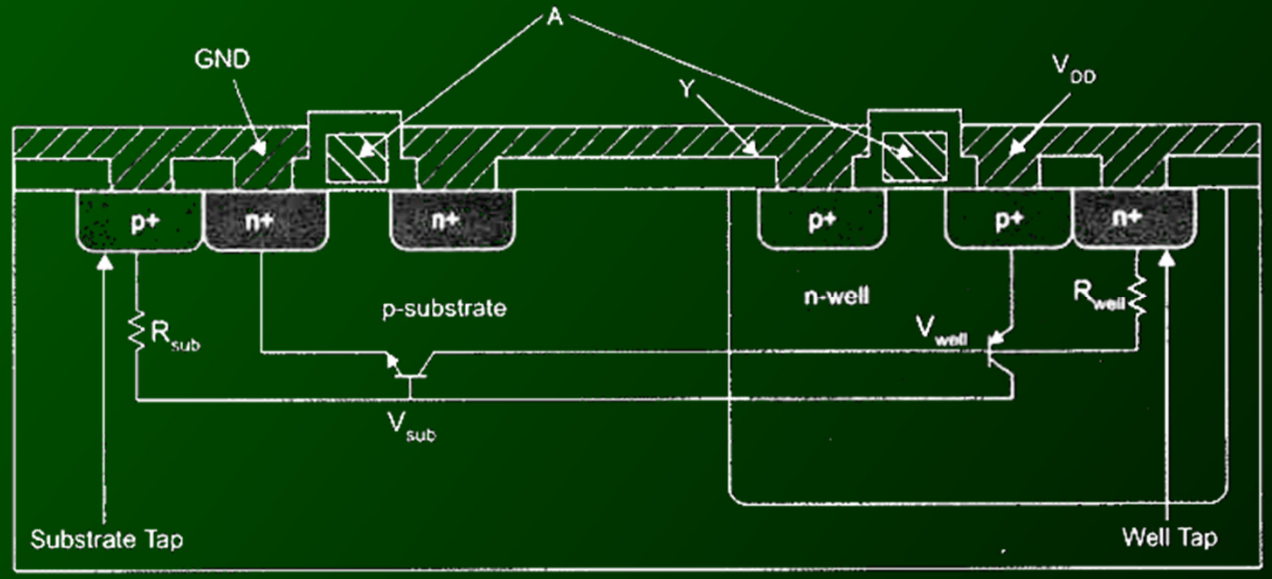
Fully depleted (FD) : silicon film is thin enough that the entire film is depleted before the threshold condition is reached

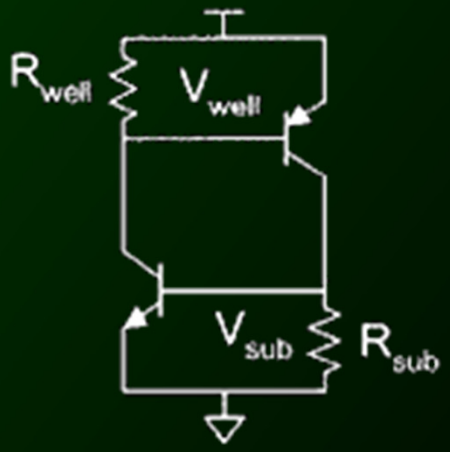
Floating-body effects:

Unique kink effect: impact ionization near the drain
→ affect the device threshold voltage
practical switching: drain current overshoot.

(Even though floating-body effects tend to enhance circuit speed in certain conditions, the drain current overshoot (or undershoot) is history dependent)

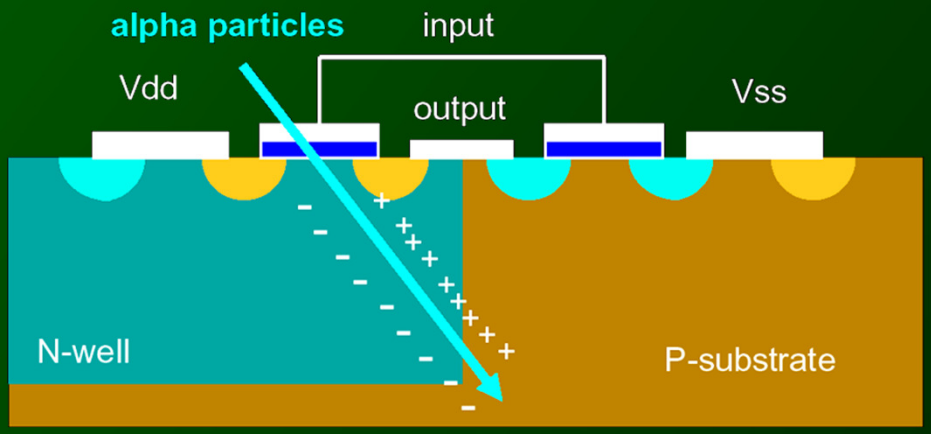
CMOS Latchup

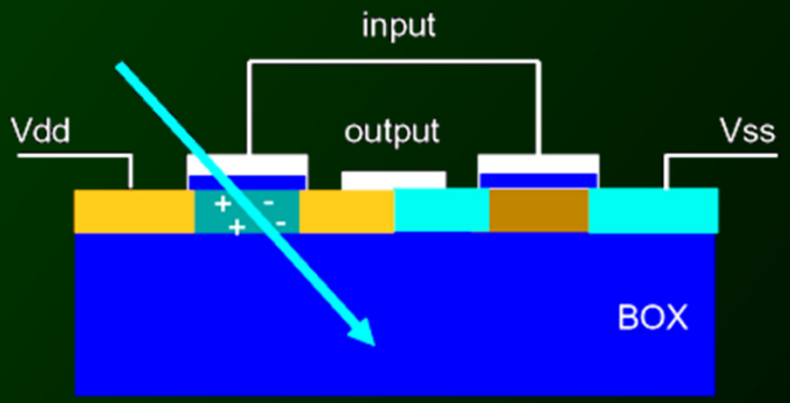




SOI : no parasitic bipolar device → no latch up

Soft Errors in bulk CMOS





Alpha Particles

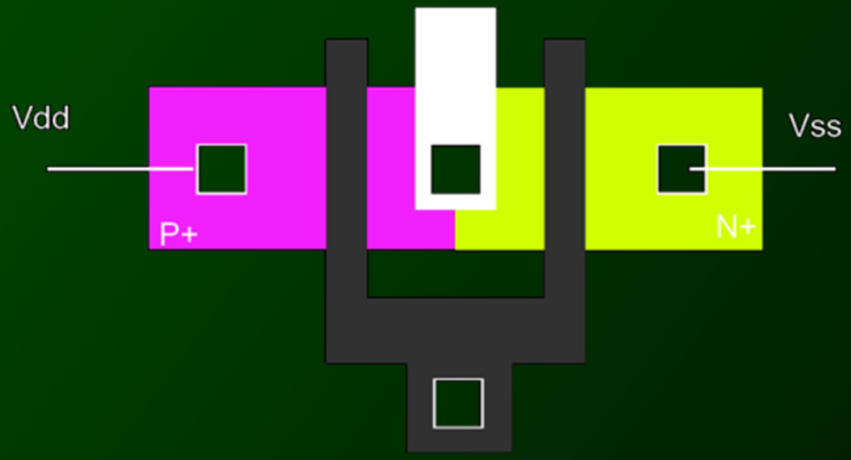
Sources:

- Cosmic Rays (aircraft electronics vulnerable)
- Decaying uranium and thorium impurities in integrated circuit interconnect

Generates electron-hole pairs in substrate:

- Excess carriers collected by diffusion terminals of transistors
- Can cause upset of state nodes – floating nodes, DRAM cells most vulnerable

Denser Layout



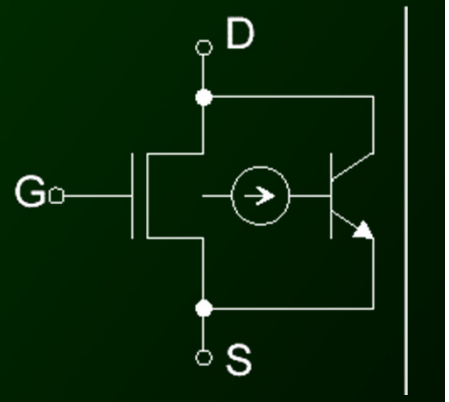
Simpler isolation → smaller layout

memory cell implementation

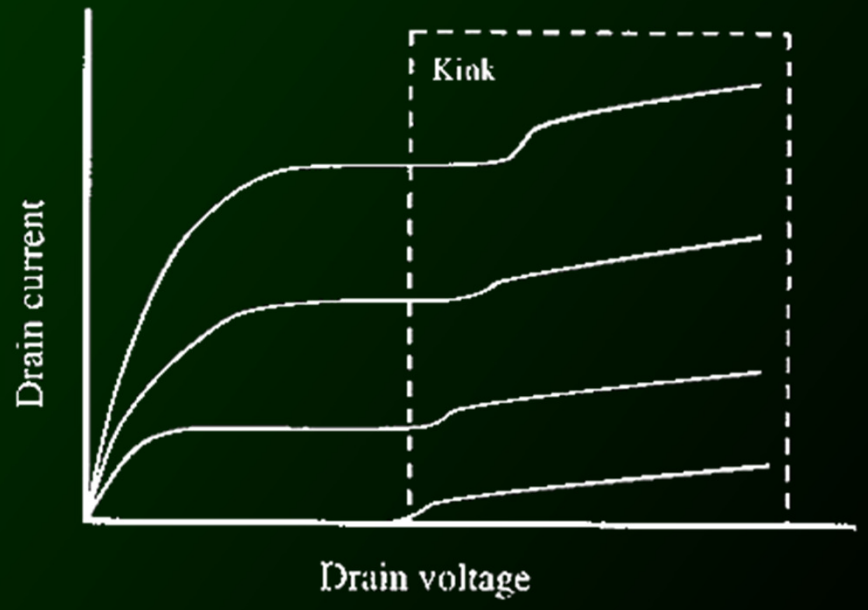
Electrical Anomalies

Floating-body effect:
Usually seen in Partially-Depleted devices.

As shown in figure, the MOS structure is accompanied by a parasitic bipolar device in parallel.The base of this device is 'floating'.



Kink Effect:
Sudden discontinuity in drain current.
Seen when the device is biased in the saturation region. The bipolar device is turned on.



Solution:

- Provide a body contact for the device.
- Use FD devices.

Q? 1/f Noise in SOI NFET

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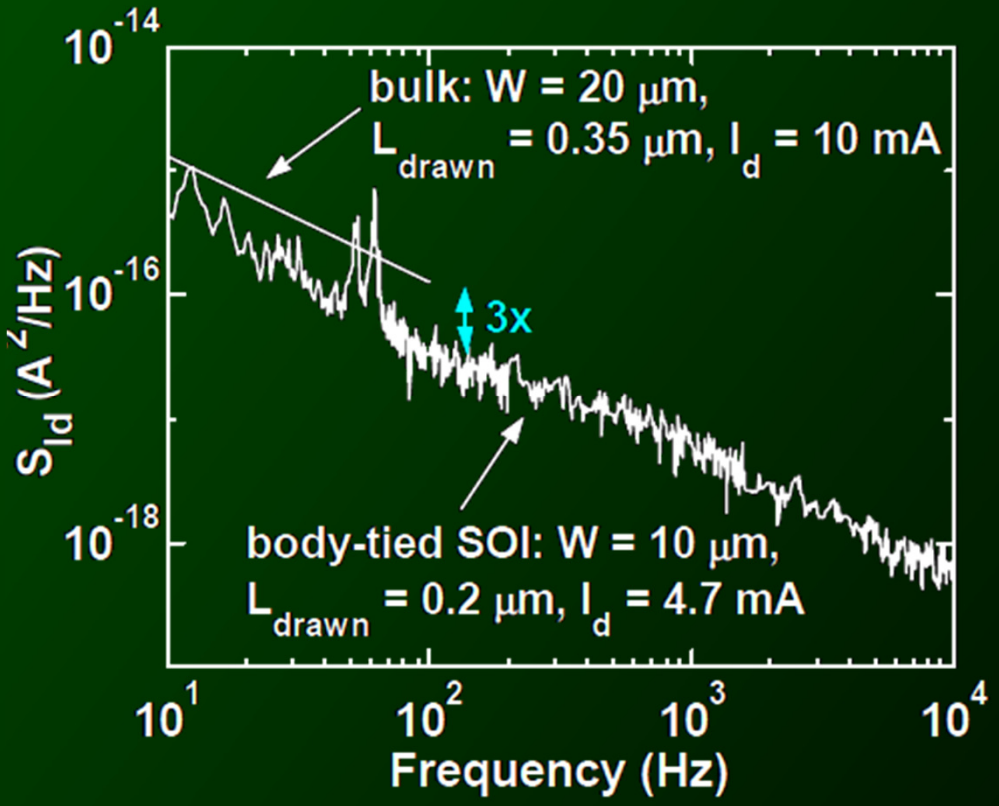

SOI offers 33% less noise than bulk.

Performance Enhancement

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Table 5.4 Components of C_{in} and C_{out}

Component	Input Capacitance (%)	Output Capacitance (%)
Intrinsic gate oxide capacitance	49	18
Overlap capacitance	51	26
Junction capacitance (nonfolded)	–	56

$$\tau = R_D(C_{out} + FO \times C_{in} + C_L)$$

Fully Depleted SOI MOSFETs

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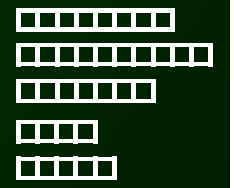

Floating-body effect can be largely avoided in FD SOI devices

the entire silicon film can be undoped because FD SOI MOSFETs scale by the silicon film thickness

$$m = 1 + \frac{C_{dep}}{C_{Ox}} = 1 + \frac{3t_{Ox}}{W_T} \approx 1$$

lower V_T (for the same off-current) → lower supply voltages → low power operation

To function properly:

$$L_{min} \sim 4.5(t_{Si} + 3t_{Ox}) \quad \sim 0.5 \; L_{\min_{Bulk}}$$

Thin-Silicon SOI Bipolar

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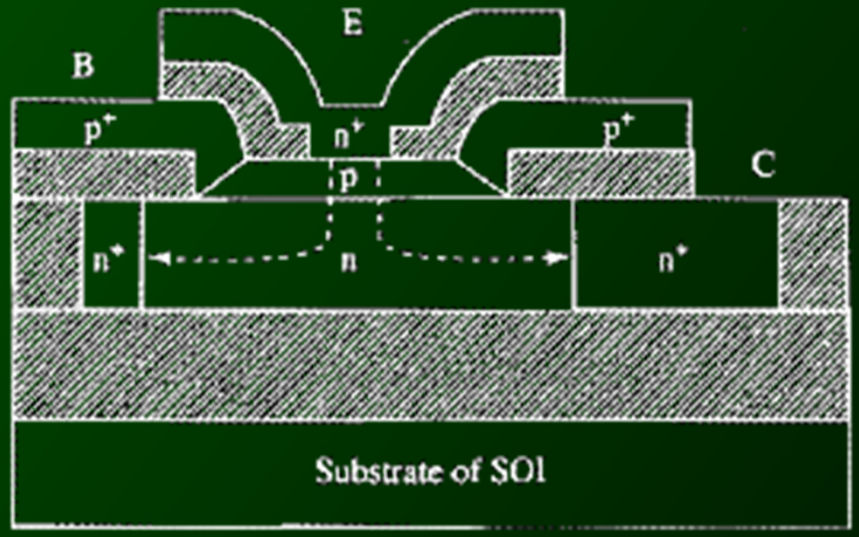
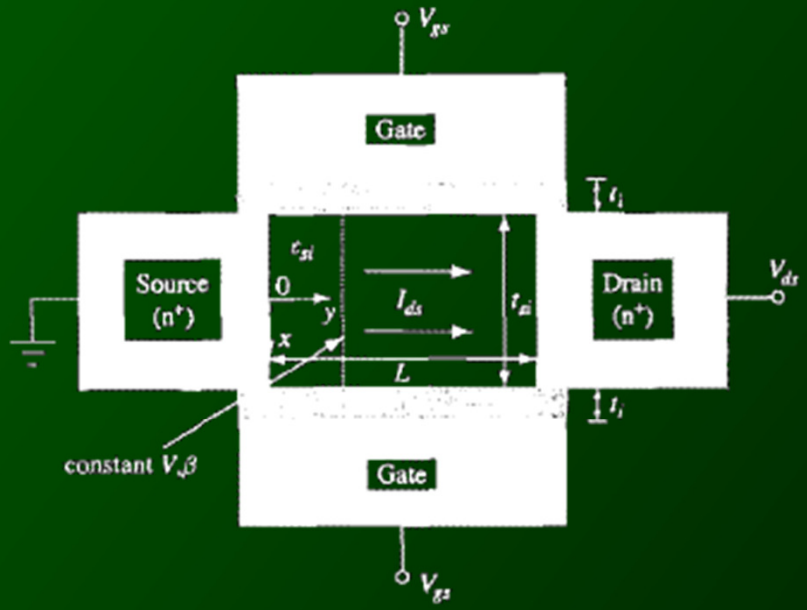
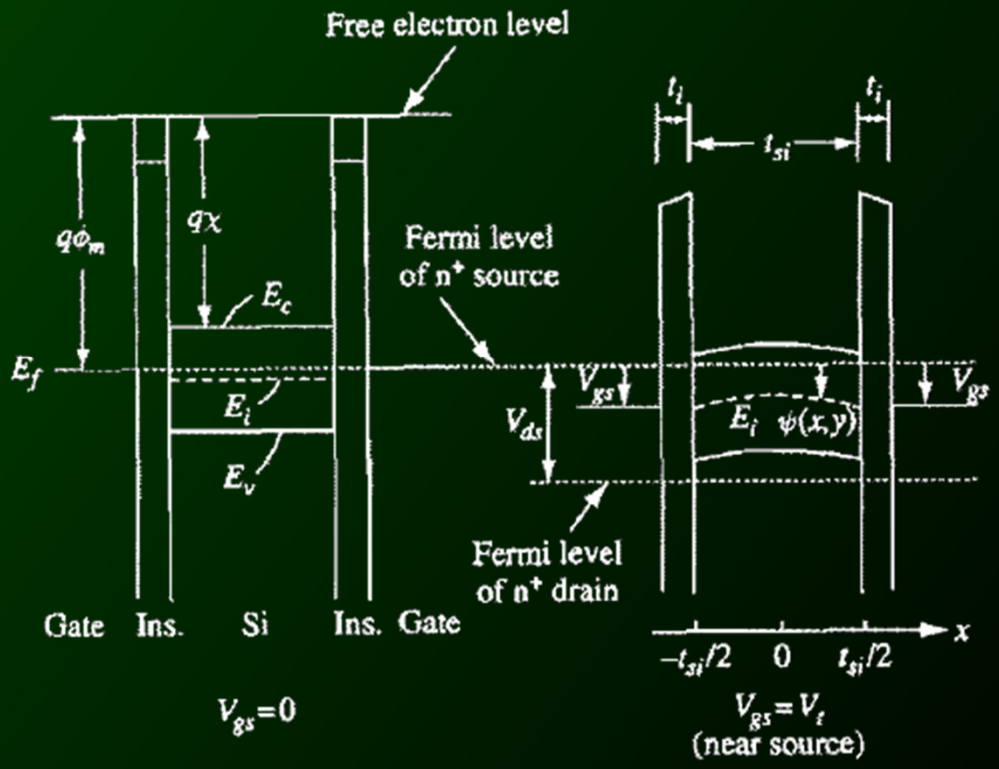


Schematic cross section of a thin-silicon SOI SiGe-base bipolar transistor. The dotted arrows indicate the path ofelectrons from the emitter to the collector reach-through.

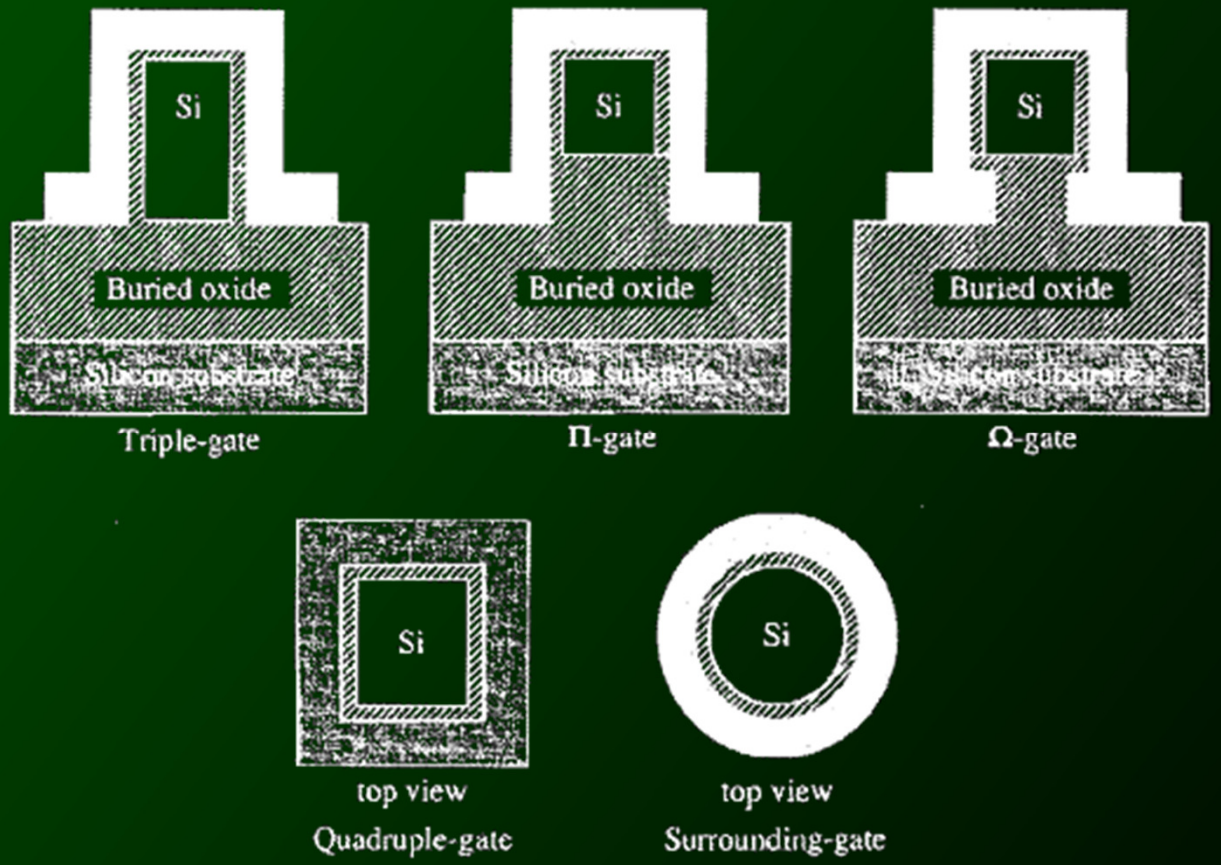
Double-Gate MOSFETs





$$L_{min} \sim 1.5(t_{Si} + 2t_{Ox})$$

Multiple-Gate MOSFETs



Scaling Limits!

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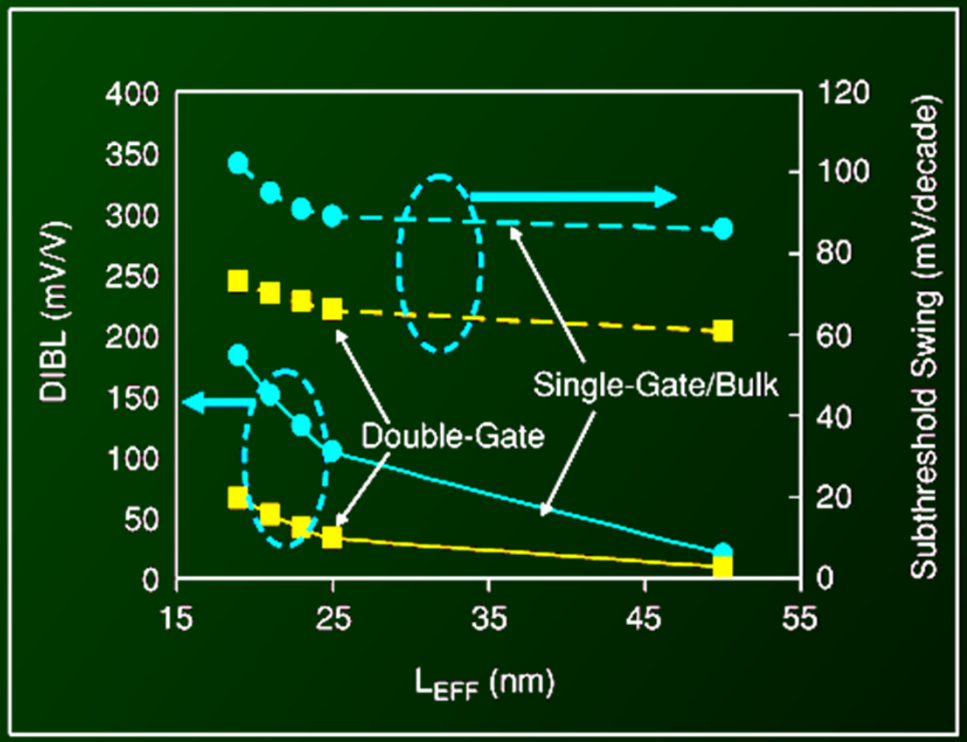
Table 1.2 Characteristic scale length for thin film transistor architectures (From [9–12])

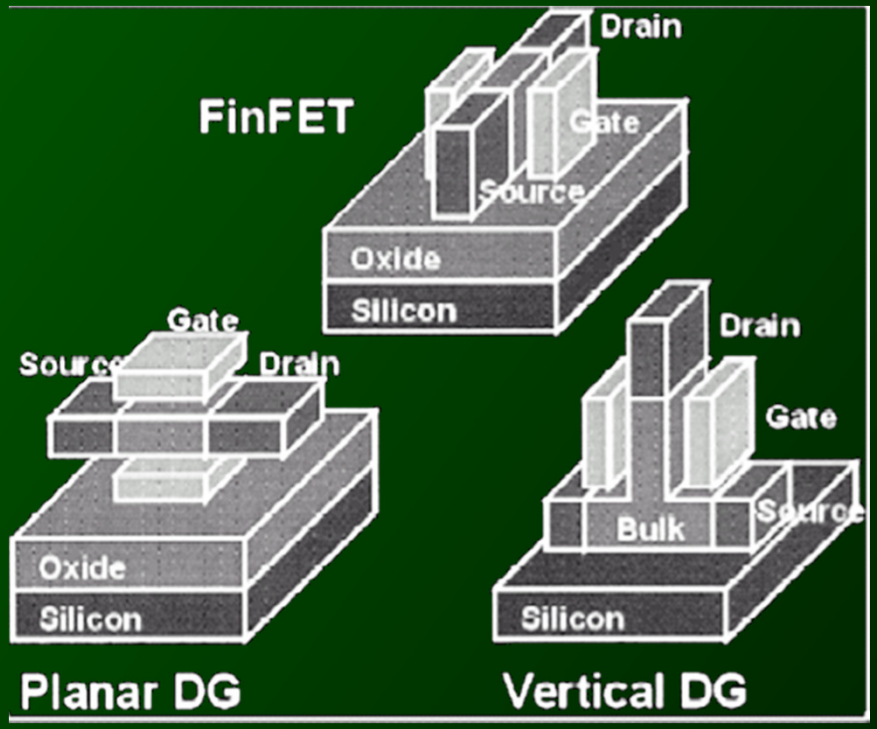
Device architecture	Scale length	Minimum channel length for $t_{Si} = 5\,nm$, EOT = 0.8 nm
Single gate FDSOI	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} \left(t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{t_{Si}}{2} \right)}$	22 nm
Double gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} \frac{t_{Si}}{2} \left(t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{t_{Si}}{4} \right)}$	13 nm
Surrounding channel	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} \frac{t_{Si}}{4} \left(\frac{t_{Si}}{2} \ln \left(1 + \frac{2t_{ox}}{t_{Si}} \right) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{t_{Si}}{4} \right)}$	9 nm

DG SOI



Medici-predicted DIBL and subthreshold swing versus effective channel length for DG and bulk-silicon nFETs

FINFET


FinFET
Drain
Gate
Source
Oxide
Silicon
Gate
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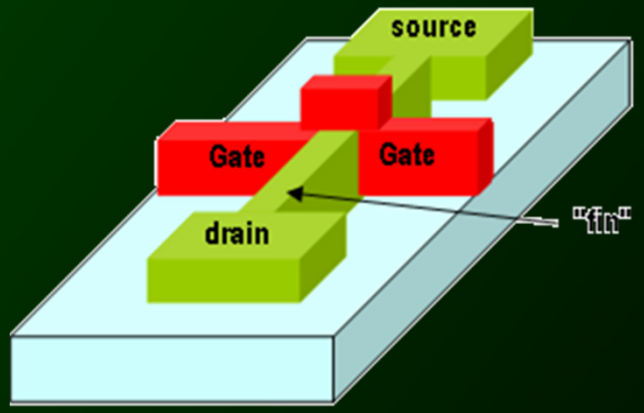
Silicon
Drain
Gate
Bulk
Source
Silicon
Planar DG
Vertical DG


source
Gate
Gate
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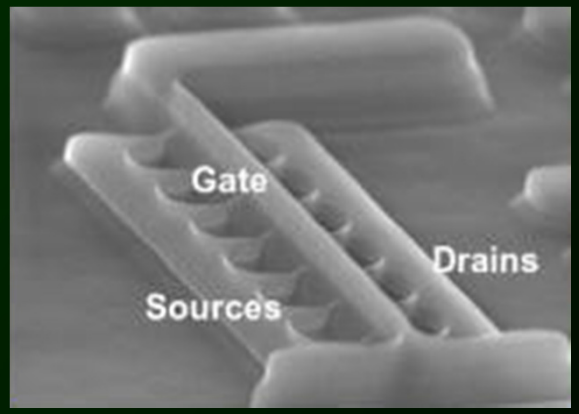
"fin"


Gate
Drains
Sources

FINFET

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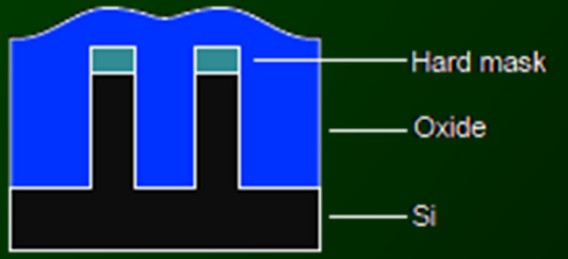
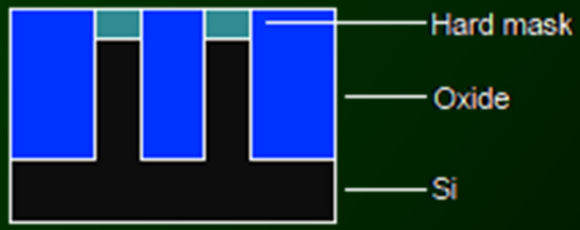
lightly p-doped substrate with a hard mask on top (e.g. silicon nitride) as well as a patterned resist layer

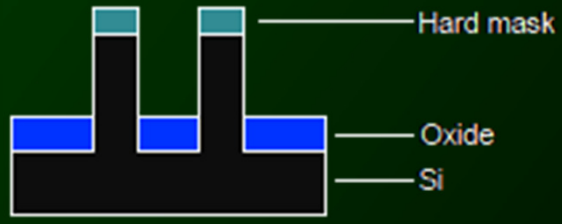
highly anisotropic etch process(height ~ 2.width)

oxide deposition with a high aspect ratio filling

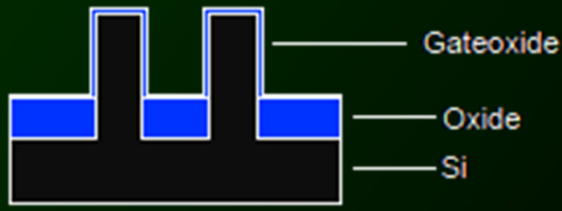


oxide is planarized by chemical mechanical polishing

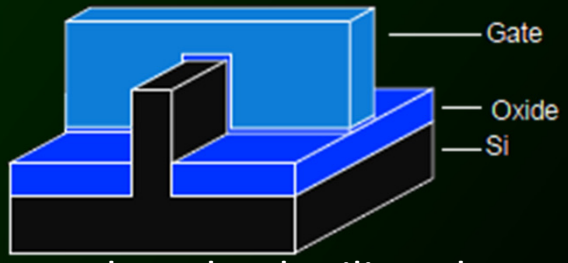




Another etch process is needed to recess the oxide film to form a lateral isolation of the fins



gate oxide is deposited via thermal oxidation



highly n+ doped poly silicon layer is deposited

Q? Punch through in SOI

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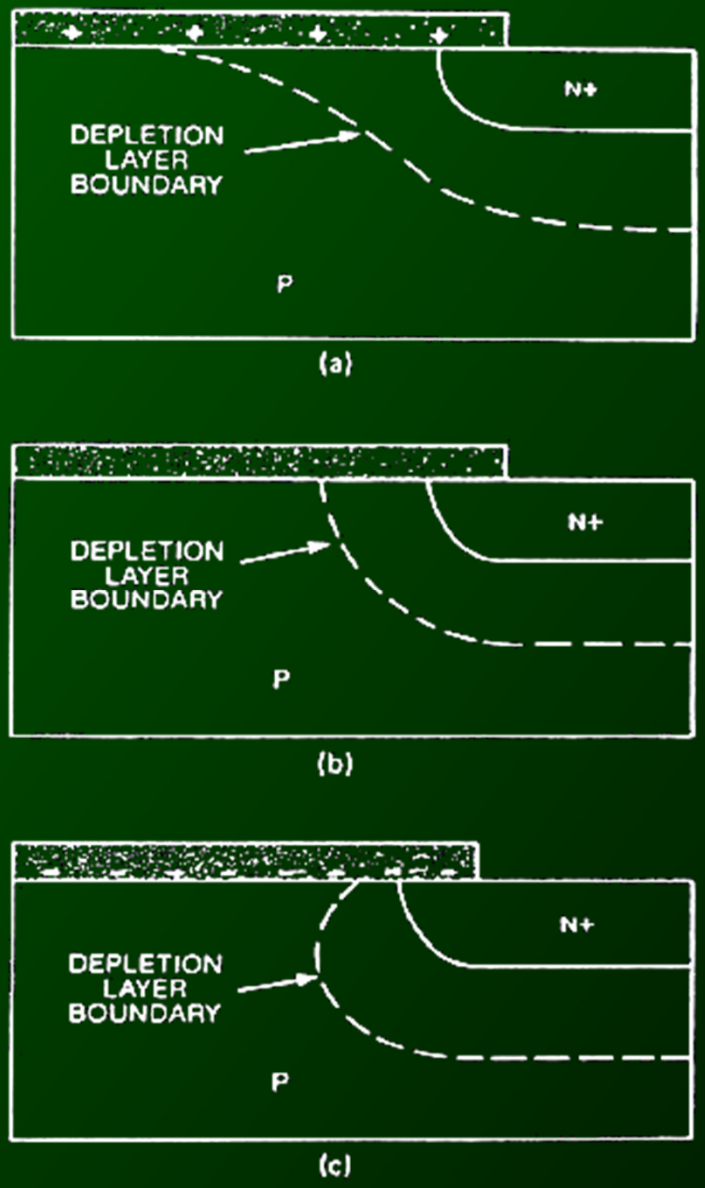

Surface charge influence on the depletion layer at the edge of a planar junction:

(a) positive charge
(b) zero charge
(c) negative charge

Strained Si

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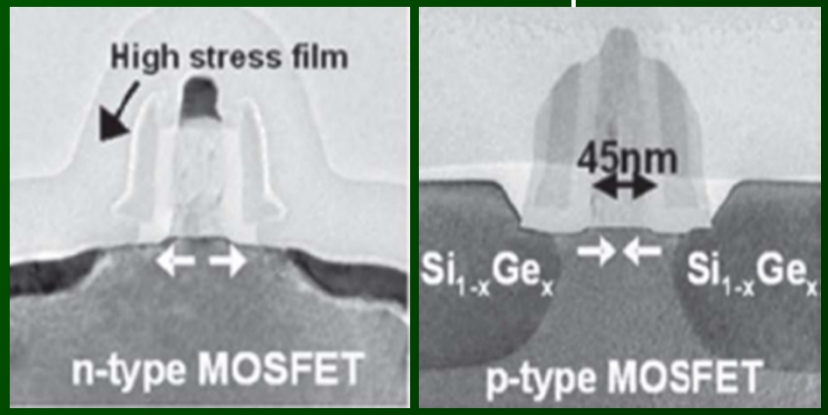
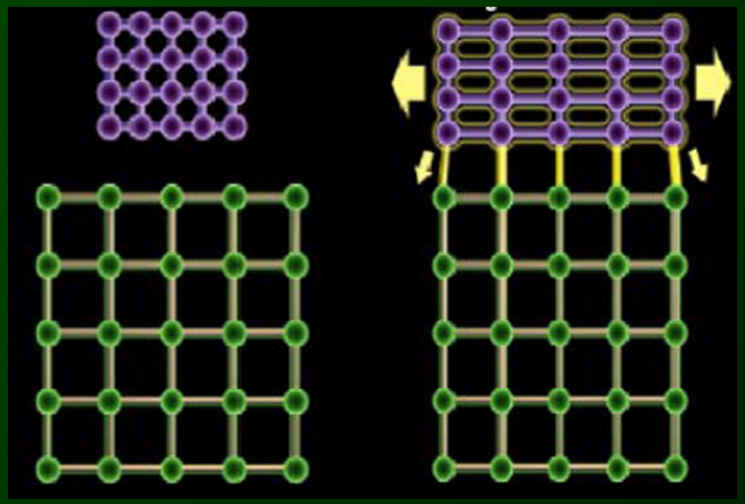
tension compression



IEEE ED, Vol 25, pp 191.



$$\mu = \frac{q\tau}{m^*}$$

Lattice Mismatch!

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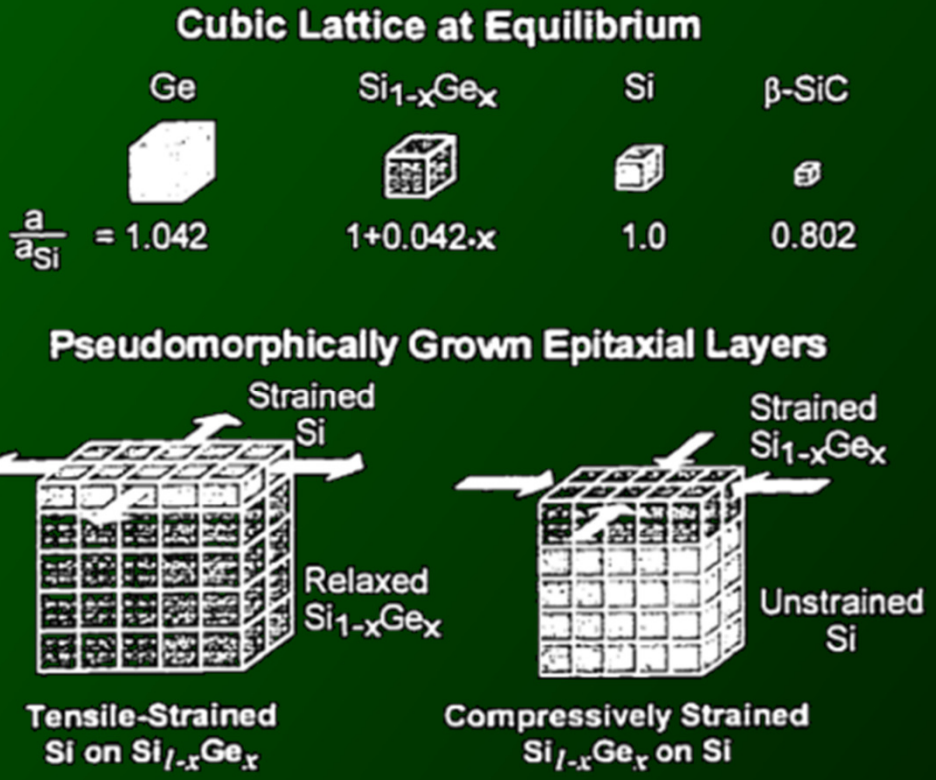
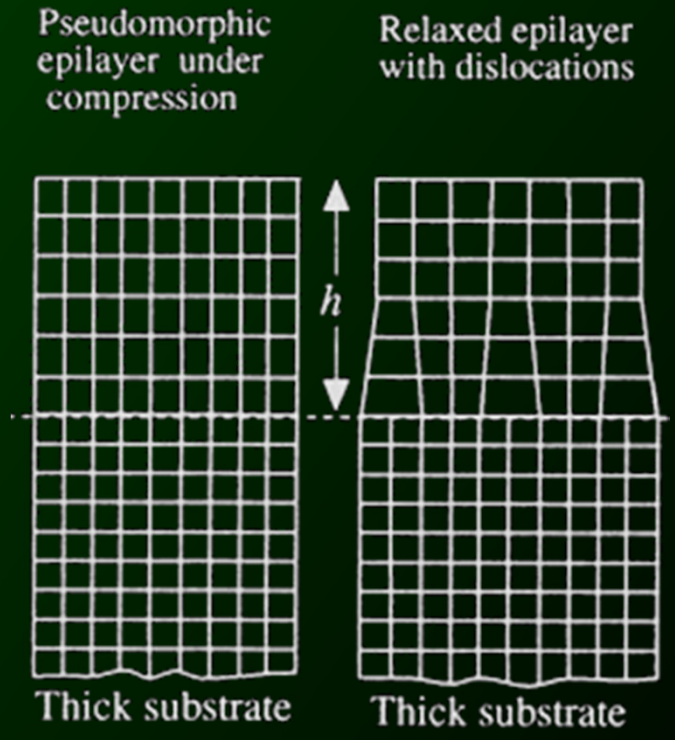
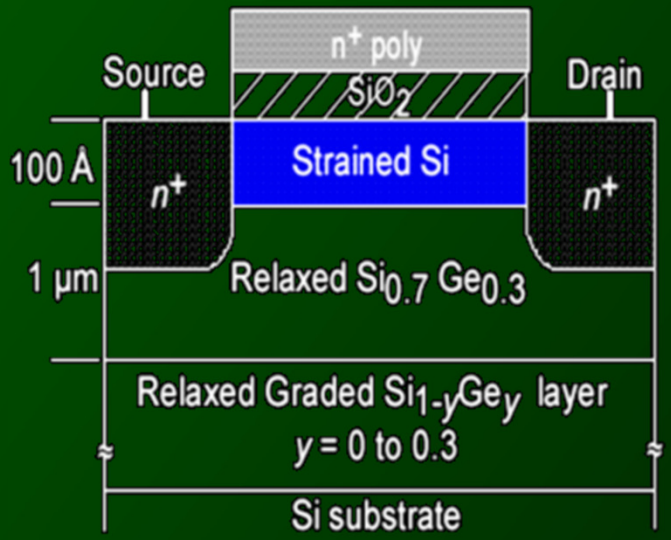
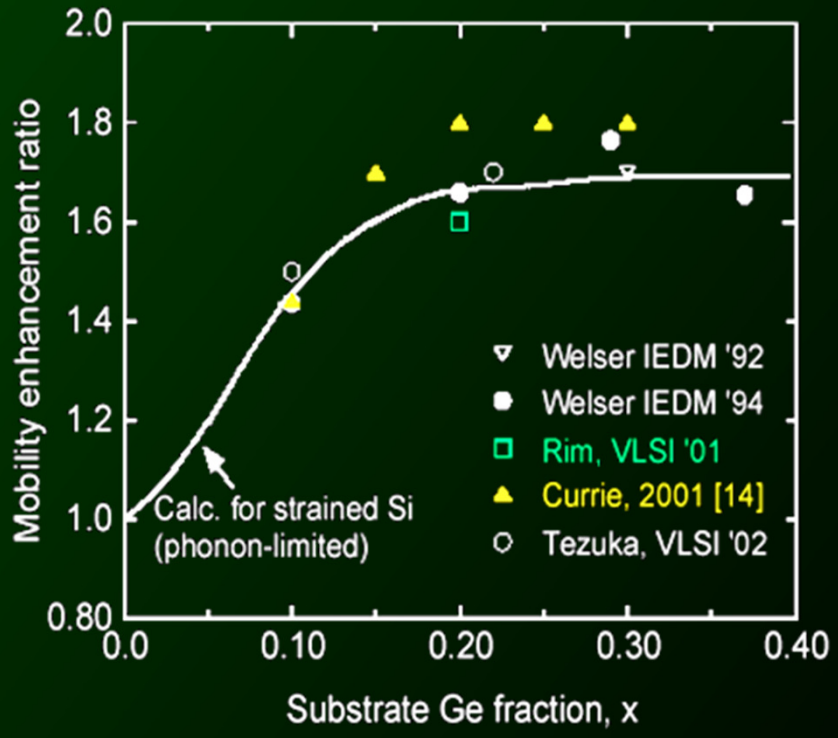


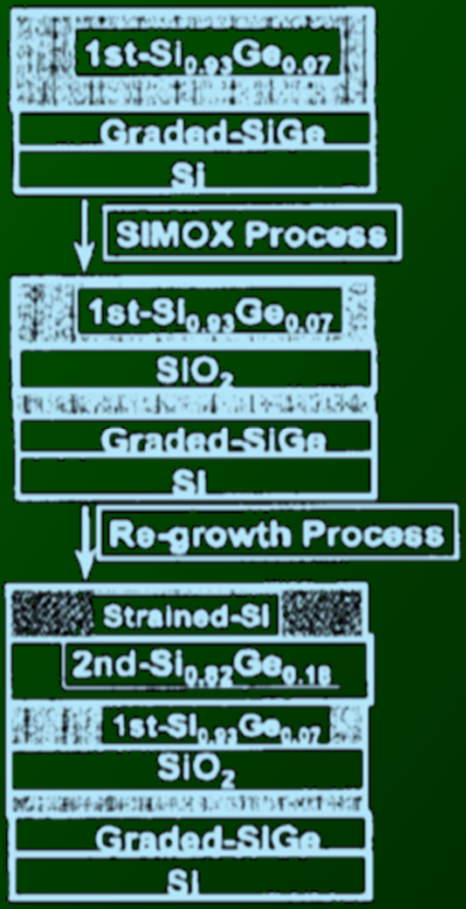


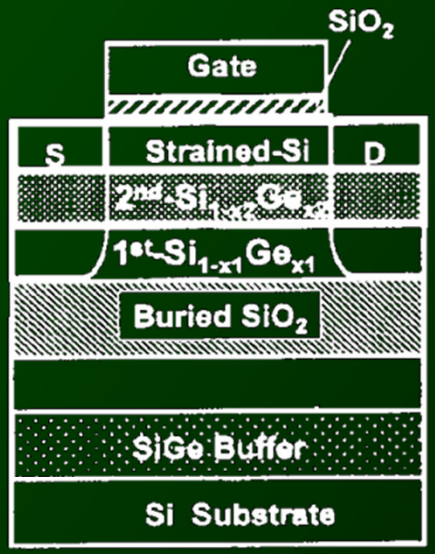
Strained Si n-MOSFET



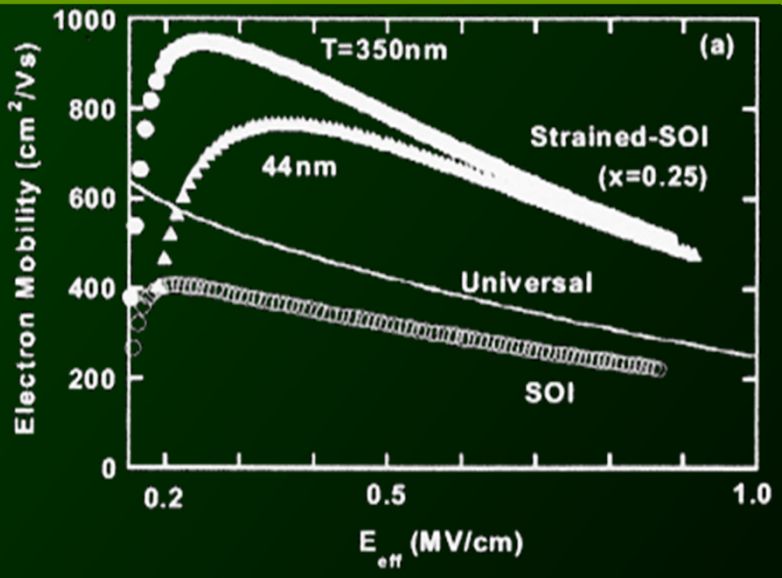


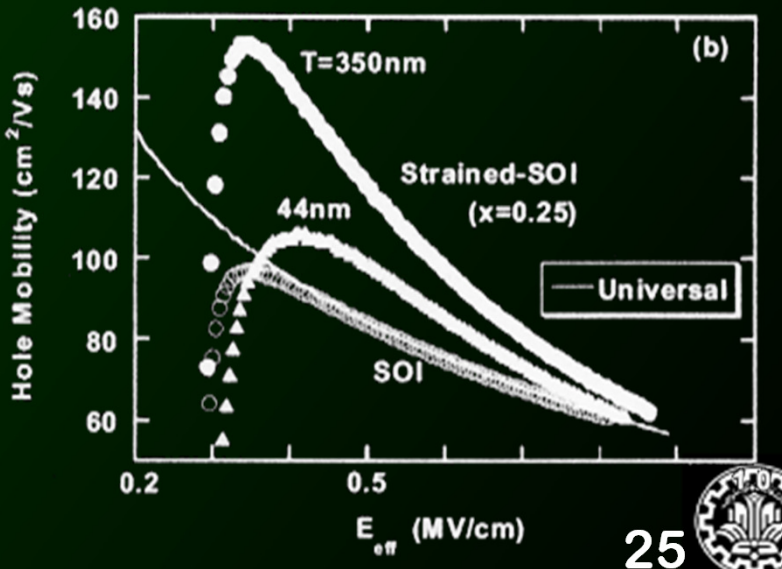
Strained Silicon in SOI



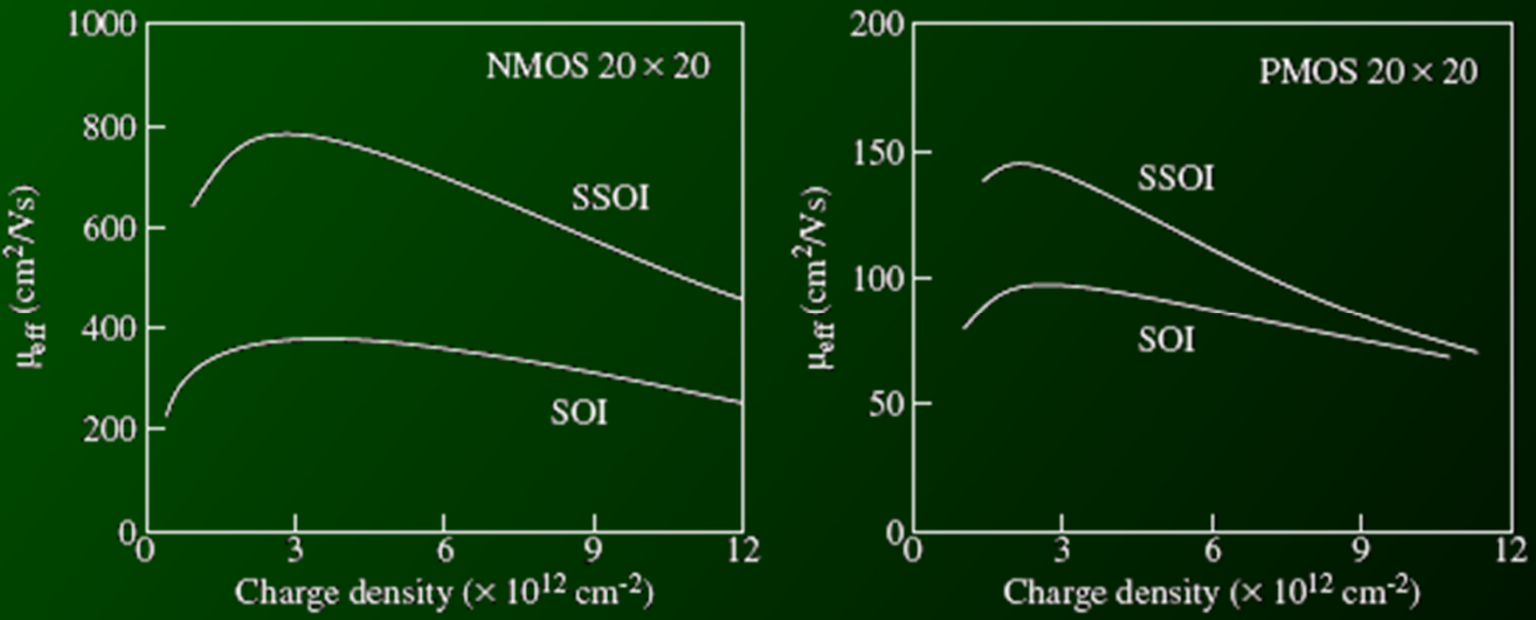


Peak electron mobility enhancement = 85%
Peak hole mobility enhancement = 50%





SSOI vs. SOI



Charge mobility enhancement of SSOI vs. SOI

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