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Design of n-Tier Multilevel Interconnect Architectures by Using Carbon Nanotube Interconnects

Esmat Kishani Farahani, *Member, IEEE*, and Reza Sarvari, *Member, IEEE*

***Abstract*— In this paper, n-tier methodology is developed to design multilevel interconnect architecture of macrocells using single-wall carbon nanotube (SWCNT) bundles. Upper limit of low-bias voltage of SWCNT bundle interconnects is derived and its dependence on temperature, SWCNTs' diameter, and interconnect length is studied. Possibility of using SWCNT bundles as local interconnects at 7.5-nm technology node is discussed, and it is shown that SWCNT bundles with 1 nm diameter cannot be used at the first interconnect metal level. Using Cu and SWCNT bundles, multilevel interconnect architecture of a 7.5-nm ASIC macrocell is designed which reduces the number of metal levels by 27% and power dissipation by 25% compared with the multilevel interconnect architecture designed with only Cu. The effect of aspect ratio (AR) on the n-tier design is studied. It is shown that decreasing AR of SWCNT bundle interconnects, decreases total power dissipation of the ASIC macrocell by 41%. The impact of temperature variation on the design of multilevel interconnect architecture is also investigated.**

***Index Terms*— Carbon nanotube (CNT), low-bias regime, multilevel interconnect architecture, n-tier methodology, temperature variation.**

I. Introduction

Carbon nanotubes (CNTs) are promising candidates to replace copper interconnects [1]–[3]. They have outstanding properties such as long mean-free path [4], high thermal conductivity [5], and high current-carrying capability [6] that outperform copper interconnects. One of the challenges to implement CNT bundle interconnects on chips, has been the production of dense vertical and horizontal CNT bundles with suitable lengths, widths, and thicknesses to be integrated into CMOS technologies. Fabrication of dense vertical CNT bundles as vias is reported in [7]–[9]. Although fabrication of horizontal CNT bundles is more challenging, Chiodarelli *et al*. [10] have reported their fabrication with dimensions down to 50 nm and symmetrical contacts. Moreover, dense horizontal CNT bundles over 100-μm length are fabricated using liquid-assisted flattening technique [11].

Although technology is going toward replacing Cu interconnects with CNT bundles, there is no clear image of chips designed with CNT bundle interconnects and their differences with the conventional chips from the viewpoint of interconnect power dissipation, repeater power dissipation, wire pitch, and number of metal levels. In this paper, n-tier methodology [12] is developed to design multilevel interconnect architectures by using CNT bundles. Maximum allowed low-bias voltage for CNT bundles is derived and the influence of temperature, CNTs' diameter, and interconnect length on the low-bias voltage is studied. Possibility of using CNT bundles as local interconnects at 7.5-nm technology node is discussed. Multilevel interconnect architecture of an ASIC logic macrocell case study for 7.5-nm technology node is designed with Cu and CNT bundles. Impact of CNT bundles' aspect ratio (AR) on the n-tier design is investigated. Multilevel interconnect architecture of the macrocell is designed for different temperatures and the results are compared.

This paper is organized as follows. In Section II, n-tier methodology is developed for CNT bundle interconnects. In Section III, upper limit of low-bias voltage for CNT bundles is derived and possibility of using CNT bundles as local interconnects for the 7.5-nm technology node is discussed. In Section IV, multilevel interconnect architecture for a 7.5-nm ASIC macrocell is designed using Cu and CNT bundles and the results are compared. In Section V, impact of CNT bundles' AR on multilevel interconnect architecture design of the macrocell is studied. In Section VI, multilevel interconnect architecture of the macrocell is designed for different temperatures, and the impact of temperature variation on the design is discussed. Section VII concludes the paper.

II. Development of n-Tier Methodology for CNT Bundles

In the n-tier method [12], the stochastic wire-length distribution [13] is used to design wire pitch of each tier optimally by considering area and time constrains. Two adjacent orthogonal metal levels are called a pair, and a collection of pairs with the same wire pitch is called a tier (Fig. 1). The area constrain is considered by equating available area for wiring A_{av} to required area for wiring A_{req} as [12]

$$A_{\mathrm{av}} = e_w A_m = \chi p_t \sqrt{\frac{A_m}{N_g}} \int_{L_{\min}^t}^{L_{\max}^t} l i(l) dl = A_{\mathrm{req}} \qquad (1)$$

where e_w is the wiring efficiency (40%), A_m is the macrocell area, χ is the point to point conversion factor [13], p_t is the wire pitch of tth pair, N_g is the number of logic gates,

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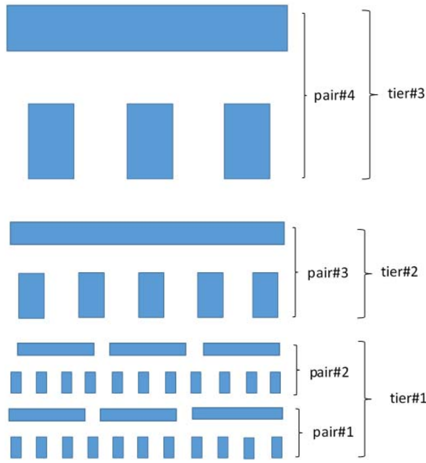

Fig. 1. n-tier multilevel interconnect architecture.

$L_{\min}^t$ and $L_{\max}^t$ are, respectively, minimum and maximum wire length of the tth pair in gate pitches (GPs), l is the wire length in GP, and $i(l)$ is the interconnect density function [13]. The time constrain is considered by equating delay of the longest wire in each pair τ to a fraction $\eta(=0.9)$ of the clock time $(1/f_c)$ as

$$\tau = \frac{\eta}{f_c}. \tag{2}$$

The delay of a CNT bundle interconnect with length l between two drivers with size s is as [14]

$$\tau = 0.69\left(R_{\text{out}}C_{\text{out}} + \left(\frac{R_{\text{out}}}{s} + \frac{R_Q + R_C}{2}\right)cl + \left(\frac{R_{\text{out}}}{s} + R_Q + R_C + rl\right)C_I s\right) + 0.38rcl^2 \tag{3}$$

where R_{out}, C_{out}, and C_I are, respectively, the output resistance, output capacitance, and input capacitance of the drivers with minimum size, r and c are, respectively, distributed per unit length resistance and capacitance of the interconnect, and R_Q and R_C are, respectively, quantum contact resistance and imperfect contact resistance of the CNT bundle

$$R_Q = \frac{12.9}{N_{\text{ch}}N_{\text{CNT}}} \quad [\text{k}\Omega] \tag{4}$$

$$r = \begin{cases} \frac{R_Q}{\lambda} & \text{for } l > \lambda \\ 0 & \text{for } l \le \lambda \end{cases} \tag{5}$$

$$c^{-1} = \left({c_q}^{-1} + {c_e}^{-1}\right) \tag{6}$$

$$c_q = 193.7N_{\text{ch}}N_{\text{CNT}} \quad [\text{pF}] \tag{7}$$

where λ is the mean-free path of SWCNTs, N_{ch} is the number of conducting channels per each SWCNT, N_{CNT} is the number of metallic SWCNTs in the bundle, c_e is the per unit length electrostatic capacitance of the bundle, and c_q is the quantum capacitance of the bundle [15]. Assuming the value of 10 kΩ as the imperfect contact resistance of each SWCNT, the imperfect contact resistance of the bundle is defined as $R_C = 10/N_{\text{CNT}}$ in kΩ.

Following a procedure similar to Cu interconnects, delay expression of a CNT bundle interconnect with length l, after insertion of k repeaters with size s can be stated as [16]

$$\tau = 0.69\left(\frac{R_{\text{out}}}{s}(C_{\text{out}}ks + cl + C_I sk) + \frac{R_Q + R_C}{2}(cl + 2C_I sk) + rlC_I s\right) + 0.38\frac{rcl^2}{k} \tag{8}$$

where optimal number of repeaters k_{opt} and optimal repeaters' size s_{opt} are as [16]

$$k_{\text{opt}} = \sqrt{\frac{0.38}{0.69}\frac{rcl^2}{R_{\text{out}}(C_{\text{out}} + C_I) + (R_Q + R_C)C_I s}} \tag{9}$$

$$s_{\text{opt}} = \sqrt{\frac{R_{\text{out}}cl}{(R_Q + R_C)C_I k + rlC_I}}. \tag{10}$$

It is seen that by replacing $R_Q + R_C$ with zero in (8) to (10), τ, k_{opt}, and s_{opt} of Cu interconnects are obtained.

The n-tier design starts by setting the wire pitch of the first metal pair to twice the minimum feature size of the technology. Then, maximum wire length of the pair $L_{\max}^t$ is calculated from (1). For the other pairs, (1)–(3) [or (8)] should be solved simultaneously to determine the wire pitch and the maximum wire length of each pair.

III. Upper Limit of Low-Bias Voltage for CNT Bundle Interconnects

Depending on the bias voltage applied to CNT bundle interconnects, they may work at low-bias or high-bias regime. At the low-bias regime, effective mean-free path of CNTs is limited by acoustic phonon scattering, whereas at the high-bias regime, the effective mean-free path is determined by optical phonon scattering [17]. For interconnect applications, low-bias regime is of great importance because of CNTs' linear behavior and long mean-free path. To work at low-bias regime, acoustic phonon mean-free path λ_{ac} must be much smaller than optical phonon mean-free path λ_{opt} so that λ_{ac} becomes dominant term in determining effective mean-free path (11). This can be expressed as $\lambda_{\text{ac}} = \gamma\lambda_{\text{opt}}$ [17] where γ is a criterion used to define low-bias regime, and is smaller than 1. For example, for $\gamma = 0.1$, $\gamma = 0.15$, and $\gamma = 0.3$, λ_{eff} is 0.91, 0.87, and 0.77 times of λ_{ac}, respectively. So $\gamma = 0.1$ shows a low-bias regime well, however, by increasing γ the approximation of low-bias regime becomes weaker

$$\lambda_{\text{eff}} = \left(\frac{1}{\lambda_{\text{ac}}} + \frac{1}{\lambda_{\text{opt}}}\right)^{-1}. \tag{11}$$

Optical phonon mean-free path is defined as [18]

$$\lambda_{\text{opt}} = \left(\frac{1}{\lambda_{\text{op,abs}}} + \frac{1}{\lambda_{\text{op,ems}}^{\text{fld}}} + \frac{1}{\lambda_{\text{op,ems}}^{\text{abs}}}\right)^{-1} \tag{12}$$

where $\lambda_{\text{op,abs}}$ is optical phonon absorption mean-free path. $\lambda_{\text{op,ems}}^{\text{fld}}$, and $\lambda_{\text{op,ems}}^{\text{abs}}$ are optical phonon emission mean-free paths due to electric field and absorption, respectively.

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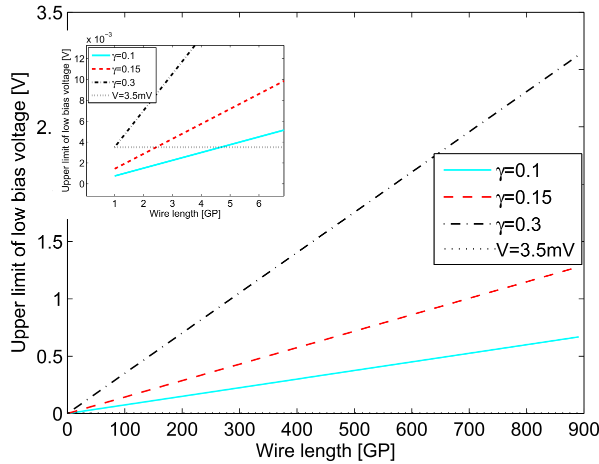

Fig. 2. Upper limit of low-bias voltage versus wire length for CNTs with 1 nm diameter and for three different criteria at room temperature. Inset: magnified plot for short-length wires.

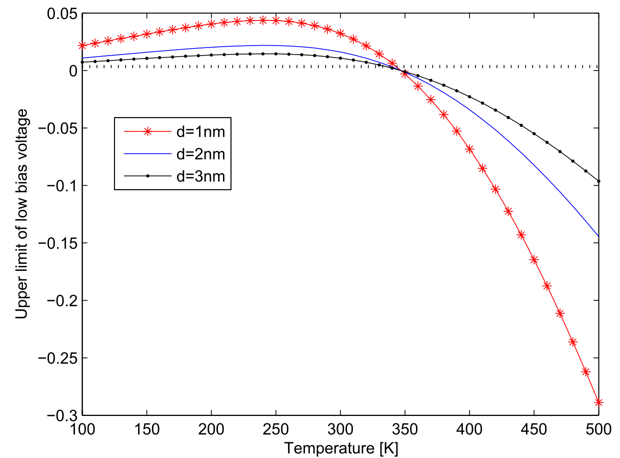

Fig. 3. Upper limit of low-bias voltage versus temperature for CNTs with 1 nm diameter and for three different criteria, $L = 43$ GP. Dotted line: $V_{\max} = 3.5$ mV.

The formulas of the mean-free paths are given in [18] that can be rewritten as

$$\lambda_{\mathrm{ac}} = 4 \times 10^5 \frac{d}{T} \tag{13}$$

$$\lambda_{\mathrm{op,abs}} = \alpha d \left(e^{\frac{\hbar\omega_{\mathrm{op}}}{K_B T}} - 1 \right) \tag{14}$$

$$\lambda_{\mathrm{op,ems}}^{\mathrm{abs}} = 2\alpha d \sinh\left(\frac{\hbar\omega_{\mathrm{op}}}{K_B T} \right) \tag{15}$$

$$\lambda_{\mathrm{op,ems}}^{\mathrm{fld}} = \frac{\hbar\omega_{\mathrm{op}} - K_B T}{qV} L + \alpha d \left(1 - e^{-\frac{\hbar\omega_{\mathrm{op}}}{K_B T}} \right) \tag{16}$$

where d is the SWCNTs' diameter, T is the temperature, $\hbar\omega_{\mathrm{op}} = 0.18$ eV, $\alpha = 56.0531$, and K_B is the Boltzmann constant. Substituting (13)–(16) in $\lambda_{\mathrm{ac}} = \gamma\,\lambda_{\mathrm{opt}}$ and solving for V, upper limit of low-bias voltage is derived as

$$V_{\mathrm{UL}} = \frac{(\hbar\omega_{\mathrm{op}} - K_B T)L}{qd\left[\alpha\left(e^{-\frac{\hbar\omega_{\mathrm{op}}}{K_B T}} - 1 \right) + \frac{1}{\zeta} \right]} \tag{17}$$

$$\zeta = 2.5 \times 10^{-6} \gamma\, T - \frac{e^{-\frac{\hbar\omega_{\mathrm{op}}}{K_B T}}}{2\alpha \sinh\left(\frac{\hbar\omega_{\mathrm{op}}}{2K_B T} \right)} - \frac{1}{2\alpha \sinh\left(\frac{\hbar\omega_{\mathrm{op}}}{K_B T} \right)}. \tag{18}$$

As (17) shows, upper limit of low-bias voltage V_{UL} is a function of wire length, SWCNTs' diameter, and temperature. V_{UL} is proportional to wire length and reciprocal of SWCNTs' diameter, whereas its dependence on temperature is not simply distinguishable.

Fig. 2 shows V_{UL} versus wire length for CNTs with 1 nm diameter and for three different criteria ($\gamma = 0.1$, 0.15, and 0.3) at room temperature. It is seen that V_{UL} increases by wire length. So, if the smallest wire length (1 GP) on a macrocell works at low-bias regime for a technology node, definitely the other wire lengths of the macrocell will work at the low-bias regime too. So we consider an 1 GP interconnect (1 GP = 0.1178 μm for 7.5-nm technology node [19]) between two drivers and investigate its V_{UL}. According to [20], maximum voltage that drops on the interconnect for the worst case is as

$$V_{\max} = \frac{(R_C + R_Q)}{(R_C + R_Q) + R_{\mathrm{out}}} V_{\mathrm{dd}}. \tag{19}$$

For a SWCNT bundle interconnect (wire pitch = 15 nm, length = 1 GP, aspect ratio = 2.1, diameter of SWCNTs = 1 nm) in the 7.5 technology node, $R_Q = 83.8\ \Omega$ and $R_C = 130\ \Omega$, also $R_{\mathrm{out}} = 36.86$ kΩ and $V_{\mathrm{dd}} = 0.61$ V [19] that result in $V_{\max} = 3.5$ mV. It is seen that $V_{\max}$ is much smaller than V_{dd} because of the significant output resistance of the drivers. Assuming only one third of the SWCNTs in the bundle to be metallic, $V_{\max}$ becomes 10.4 mV.

As the inset of the Fig. 2 shows V_{UL} of 1 GP wire length is 0.75 mV for $\gamma = 0.1$ which is smaller than $V_{\max}$, whereas for wire lengths larger than 4 GP, $V_{\max} < V_{\mathrm{UL}}$. So, we do not use CNTs for wiring the first metal pair. We also do not use two different kinds of interconnect for wiring a pair, because its implementation may be difficult technologically.

Fig. 3 shows dependence of V_{UL} on temperature for CNTs with 1 nm diameter and for three different criteria. The length of CNTs is 43 GP (minimum wire length in pair 2 according to the next section). The dotted line shows $V_{\max} = 3.5$ mV. For the temperatures that V_{UL} becomes smaller than $V_{\max}$, the assumption of low-bias regime is not valid. In other words, this temperature range represents high-bias regime in which optical phonons determine effective mean-free path of CNTs. As Fig. 3 shows a CNT with 1 nm diameter and 43 GP length works at the low-bias regime up to temperature $T = 343$ and 380 K for the criteria of $\gamma = 0.1$ and $\gamma = 0.15$, respectively.

Fig. 4 shows dependence of V_{UL} on temperature for CNTs with different diameters. The wire length is 43 GP and $\gamma = 0.1$. It is seen that V_{UL} decreases by increasing d. The maximum temperature for low-bias regime for CNTs with diameters 1, 2, and 3 nm is, respectively, 343, 340, and 334 K. It is also seen that the temperature at which CNTs with different diameters cross the zero voltage, is the same.

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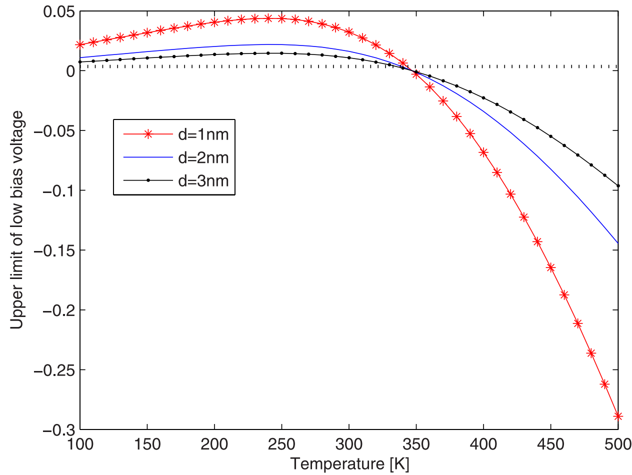

Fig. 4. Upper limit of low-bias voltage versus temperature for CNTs with 1, 2, and 3 nm diameter, $\gamma = 0.1$, $L = 43$ GP. Dotted line: $V_{\max} = 3.5$ mV.

TABLE I

DATA USED FROM ITRS FOR THE CASE STUDY

Year	2024
1/2 wiring pitch[nm]	7.5
Clock frequency f_c[GHz]	6.234
Chip area $[cm^2]$	8.58
Number of logic gates [millions]	61798
V_{dd} [V]	0.61
Subthreshold channel leakage current of NMOS transistor I_{leak} [nA/μm]	100
Threshold voltage of NMOS transistor V_{th} [V]	0.249
Short circuit current of minimum size driver I_{sc} [μA/μm]	65 [22]
Output resistance of minimum size driver R_{out}	36.86kΩ
Output capacitance of minimum size driver C_{out}	3.45 aF
Input capacitance of minimum size driver C_I	3.45 aF

TABLE II

DEFINITION OF SWCNTs AND Cu PARAMETERS

Symbol	Definition	Value
λ	mean free path of SWCNTs at 300K	1.27μm
d	diameter of SWCNTs	1 nm
AR	aspect ratio of interconnects	2.1
β	ratio of the metallic SWCNTs to all SWCNTs in the bundle	1, 1/3
ρ_0	resistivity of bulk copper (no size effect)	2.2× $10^{-8}\Omega$m
λ_{Cu}	mean free path of Cu at 300K	38 nm
Ref	reflectivity coefficient of copper	0.5
$Spec$	specularity coefficient of copper	0.5
LER	line edge roughness	40%

IV. DESIGN OF n-TIER INTERCONNECT ARCHITECTURE OF AN ASIC MACROCELL BY USING SWCNT BUNDLES AND Cu

In this section n-tier methodology and developed n-tier methodology are used to design multilevel interconnect architecture of a 7.5-nm ASIC macrocell case study by using Cu and SWCNT bundles. ITRS data for the 7.5-nm technology node is tabulated in Table I. As mentioned in previous section, we use Cu for the first metal pair and CNT bundles for the other pairs, to be sure of working at low-bias regime. Parameters of Cu and SWCNT interconnects at room temperature are tabulated in Table II. We have also used a fraction of optimal

TABLE III

RESULTS OF n-TIER DESIGN FOR A 7.5-nm ASIC MACROCELL BY USING SWCNT BUNDLES AND Cu

	CASE I Cu LER=3 nm (40%)		CASE II Cu-SWCNT β=1		CASE III Cu-SWCNT β=1/3	
Pair's number	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]
1	15	42	15	42	15	42
2	15	842	15	842	15	842
3	24.7	4706	18.1	9273	21.6	6100
4	49.1	12202	51	31083	49.6	16650
5	84.7	25240	128.5	82863	101.8	36692
6	191.8	70084			221.4	82863
7	220.7	82863				

TABLE IV

COMPARISON OF POWER DISSIPATION AND THE NUMBER OF REQUIRED METAL PAIRS IN n-TIER DESIGN OF A 7.5-nm ASIC MACROCELL BY USING SWCNT BUNDLES AND Cu

	CASE I Cu LER=3 nm (40%)	CASE II Cu-SWCNT β=1	CASE III Cu-SWCNT β=1/3
Number of pairs	6.0008	4.3752	5.3449
P_{int}[W]	33.6206	33.6213	33.621
P_{rep}[W]	59.8058	36.5135	31.1319
P_{sc}[W]	0.1026	0.0626	.0534
P_{leak}[W]	37.7132	23.0252	19.6316
P_{dyn}[W]	21.99	13.4257	11.4469
P_{tot}[W]	93.4264	70.1348	64.7528

number of repeaters $\xi = 0.4$ to decrease power dissipation, in the cost of larger delay.

Power dissipation of the interconnects and repeaters are defined as [21], [22]

$$p_{\text{int}} = \frac{1}{2}\alpha c l V_{\text{dd}}^2 f_c \quad (20)$$

$$p_{\text{rep}} = p_{\text{dyn}} + p_{\text{sc}} + p_{\text{leak}} \quad (21)$$

$$p_{\text{dyn}} = \frac{1}{2}\alpha (C_{\text{out}} + C_I) s V_{\text{dd}}^2 f_c \quad (22)$$

$$p_{\text{leak}} = \frac{3}{2} V_{\text{dd}} I_{\text{leak}} w_{\text{min}} s \quad (23)$$

$$p_{\text{sc}} = \alpha t_{\text{sc}} V_{\text{dd}} I_{\text{peak}} f_c = \alpha t_{\text{sc}} V_{\text{dd}} I_{\text{sc}} w_{\text{min}} s f_c \quad (24)$$

$$t_{\text{sc}} \approx \frac{V_{\text{dd}} - 2V_{\text{th}}}{V_{\text{dd}}} \times \frac{0.69 C_{\text{out}} R_{\text{out}}}{0.8} \quad (25)$$

where p_{int} is the switching power dissipation of an interconnect with length l, α is the switching factor and is assumed to be 0.05, p_{rep} is the power dissipation of a repeater and is consisted of short-circuit power dissipation p_{sc}, leakage power dissipation p_{leak}, and dynamic power dissipation p_{dyn}, w_{min} is the minimum feature size of the technology, I_{leak} is the subthreshold channel leakage current of nMOS transistor and it is assumed to be larger than the gate and junction leakage currents [19], and t_{sc} is the time that both nMOS and pMOS transistors are on.

Tables III and IV show results of the n-tier design for three different cases. In all cases, wires have AR $= 2.1$. In CASE I, all pairs are designed with Cu. In CASE II and CASE III, pair 1 is designed with Cu and the other pairs are designed with SWCNT bundles. In CASE II, $\beta = 1$, whereas

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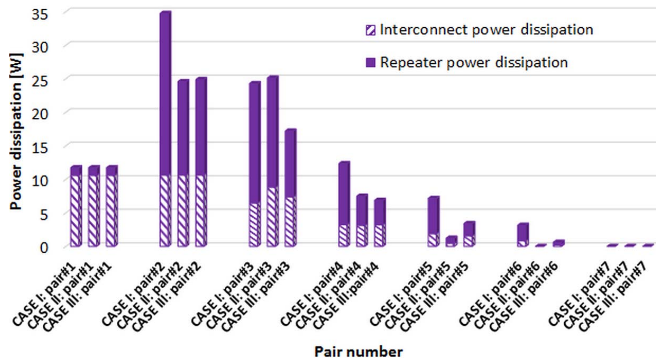

Fig. 5. Power dissipation versus pair number for the three cases.

in CASE III, $\beta = 1/3$. $L_{\max}$ represents maximum wire length in each pair. P_{int}, P_{sc}, P_{leak}, and P_{dyn} are interconnect power dissipation, short-circuit power dissipation, leakage power dissipation, and dynamic power dissipation of the macrocell, respectively. P_{rep} represents repeater power dissipation of the macrocell and is defined as $P_{\text{rep}} = P_{\text{sc}} + P_{\text{leak}} + P_{\text{dyn}}$. Total power dissipation of interconnects and repeaters is defined as $P_{\text{tot}} = P_{\text{int}} + P_{\text{rep}}$. It is seen that use of SWCNT bundles decreases the number of metal pairs, and the total power dissipation dramatically. CASE II and CASE III in comparison with CASE I show 27% and 11% reduction in the number of metal pairs, and 25% and 30% reduction in total power dissipation, respectively. Difference in power dissipation between the cases is mainly due to the difference in repeater power dissipation for which size and number of repeaters are different [refer to (22)–(24)]. Moreover, more than 60% of repeater power dissipation is due to the leakage power dissipation.

Fig. 5 shows power dissipation versus pair number for the three cases. Pair 1 of the all cases is designed with Cu, hence no difference is seen between the cases. In pair 2, the cases have equal interconnect power dissipation, because the wire pitch, minimum wire length, and maximum wire length of the cases are similar. However, their repeater power dissipations are different owing to the difference in the number of repeaters k and repeater sizes s. It is inferred from (9) and (10) that CASE II in Comparison with CASE III has smaller number of repeaters and larger repeater sizes (because r and $R_Q + R_C$ are smaller in CASE II in comparison with CASE III). The product of $s \times k$ is also larger in CASE III in comparison with CASE II that leads to larger repeater power dissipation. Repeater power dissipation of CASE I is very high in comparison with CASE II and CASE III, because of the larger product of $s \times k$. It is worthy to note that because of the nonzero value of $R_Q + R_C$ in the denominator of s_{opt} and k_{opt} for the CNT bundles, the product of $s \times k$ is smaller in comparison with Cu wires. In pair 3, the cases have different wire pitches that leads to different number of wires, interconnect power dissipations, and repeater power dissipations. CASE II in comparison with CASE III has larger interconnect and repeater power dissipation because of having larger $L_{\max}$ (Table III). For the other pairs of the cases, increasing the pair number, increases the wire pitch which causes decrease in the average wire length and consequently the interconnect

TABLE V
IMPACT OF SWCNT BUNDLES' AR ON n-TIER DESIGN FOR THE 7.5-nm ASIC MACROCELL

	Cu-SWCNT AR = 0.5		Cu-SWCNT AR = 1		Cu-SWCNT AR = 2.1	
Pair's number	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]
1	15	42	15	42	15	42
2	15	842	15	842	15	842
3	21	6486	19.3	7839	18.1	9273
4	49.7	18035	49.1	23822	51	31083
5	108	41948	160.4	82863	128.5	82863
6	207.3	82863				

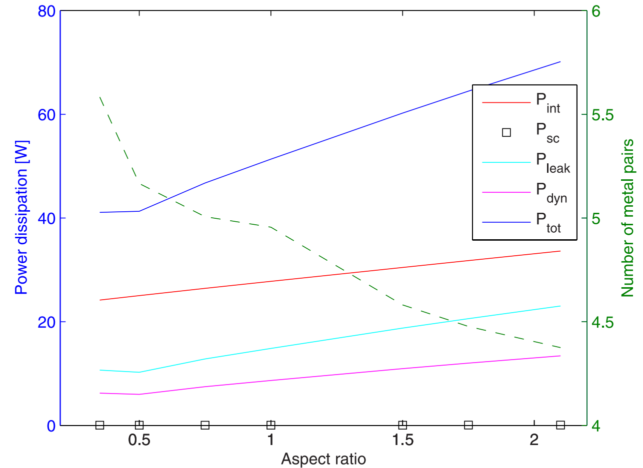

Fig. 6. Power dissipation (left axis) and number of required metal pairs (right axis) versus AR.

power dissipation. The repeater power dissipation also decreases, because although the product of $s \times k$ increases, the number of wires decreases according to the wire density function.

V. DEPENDENCE OF n-TIER DESIGN ON AR

An important feature of CNT bundle interconnects is their current-carrying capability which is three orders of magnitude larger than Cu interconnects [6]. So, one may decrease the AR of interconnects by using SWCNT bundles. This decreases capacitance per unit length of the interconnects and consequently the interconnect power dissipation. However, by decreasing AR, resistance per unit length of the interconnects increases, which may increase wire pitch of the pairs, and number of the metal pairs.

Table V shows the results of the n-tier design for the 7.5-nm ASIC macrocell case study using SWCNT bundles with different ARs. In all cases, pair 1 is designed with Cu with AR of 2.1, and the other pairs are designed with SWCNT bundles ($d = 1$ nm, $\beta = 1$). It is seen that decreasing AR, increases the number of metal pairs and the wire pitch of the pairs.

Fig. 6 shows the power dissipation and number of metal pairs versus AR. It is seen that decreasing AR from 2.1 to 0.35, decreases the total power dissipation by 41%, which means 29 W decrease in power dissipation per macrocell.

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TABLE VI
COMPARISON OF MULTILEVEL INTERCONNECT ARCHITECTURE DESIGN FOR $T = 250$, 300, AND 350 K

	Cu-SWCNT $T = 250$ K		Cu-SWCNT $T = 300$ K		Cu-SWCNT $T = 350$ K	
Pair's number	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]	pitch [nm]	L_{max} [GP]
1	15	42	15	42	15	42
2	15	842	15	842	15	842
3	17.7	9872	18.1	9273	18.5	8737
4	51.8	34963	51	31083	50.6	27977
5	116.1	82863	128.5	82863	141.5	82863

VI. TEMPERATURE VARIATION EFFECT ON n-TIER DESIGN

By technology scaling, temperature variation becomes an important issue. Borkar *et al.* [23] showed that temperature variation across a die may reach up to 50 °C. Temperature variation affects the performance of interconnects [24], so it is necessary to design multilevel interconnect architectures for acceptable performance in a temperature range. In previous sections, n-tier interconnect architectures were designed at room temperature. In this section, interconnect architecture for the macrocell is designed at $T = 250$, 300, and 350 K to investigate the impact of temperature variation on the design parameters. For Cu interconnects, temperature affects mean-free path and consequently the resistivity. Assuming electron free gas model for Cu, the product of bulk resistivity ρ_B and mean-free path λ_B is constant at all temperatures [25]

$$\rho_B(T)\lambda_B(T) = 6.6 \times 10^{-16}\ \Omega\text{m}^2. \tag{26}$$

Data for $\rho_B(T)$ is given by Matula [26], so $\lambda_B(T)$ can be computed from (26). Considering the increase in Cu resistivity due to liners, effective bulk resistivity of Cu can be obtained as

$$\rho_{\text{eff}}(T) = \frac{\rho_B(T)}{\rho_B(300)} \times (2.2 \times 10^{-8})\ \Omega\text{m}. \tag{27}$$

For CNT bundles, temperature affects mean-free path, number of conducting channels, and Fermi velocity. Temperature dependence of the mean-free path was expressed in Section III. Temperature dependence of Fermi velocity is as

$$v_f(T) = v_f(300)\sqrt{\frac{T}{300}} \tag{28}$$

where $v_f(300)$ is Fermi velocity at room temperature. Temperature dependence of number of conducting channels is stated in [27]. Table VI shows the multilevel interconnect architecture design for the 7.5-nm ASIC macrocell by using Cu and SWCNT bundles for $T = 250$, 300, and 350 K. The first pair is designed with Cu, and the other pairs are designed with SWCNT bundles ($\beta = 1$). It is seen that temperature variation does not have any effect on the wire pitch and L_{max} of pairs 1 and 2. The reason is that these pairs are limited by area. Decreasing design temperature from 300 to 250 K, decreases the wire pitch of pair 5 by 10%, and the other wire pitches remain nearly constant. Increasing the design temperature from 300 to 350 K, the wire pitch of pair 5 increases by 10%. Table VII shows power dissipation and number of metal pairs of the designs. It is seen that interconnect power dissipation does not change with temperature, whereas the number of metal pairs increases by temperature slightly. Dynamic power dissipation of the repeaters at 350 K is slightly smaller than it at 300 K because of the larger wire pitches. Decreasing the temperature from 300 to 250 K, decreases dynamic power dissipation of the repeaters by 37%, because no repeater is needed in pair 2, which is of the most power hungry pairs at higher temperatures, owing to the increase in mean-free path of CNTs by 23%. So, it can be concluded that temperature variation affects higher pairs more than lower pairs. Moreover, to mitigate its impact on interconnects performance, interconnect architectures can be designed for a higher temperature (350 K). Designing the interconnect architecture for a higher temperature, increases the number of metal pairs slightly.

TABLE VII
COMPARISON OF POWER DISSIPATION AND NUMBER OF METAL PAIRS IN MULTILEVEL INTERCONNECT DESIGN FOR DIFFERENT TEMPERATURES

	Cu-SWCNT $T = 250$ K	Cu-SWCNT $T = 300$ K	Cu-SWCNT $T = 350$ K
Number of pairs	4.2215	4.3752	4.5669
P_{int}[W]	33.6213	33.6213	33.6213
P_{dyn}[W]	8.4792	13.4257	13.3457

VII. CONCLUSION

In this paper, n-tier methodology was developed for CNT bundle interconnects. Temperature and length domain of low-bias regime for SWCNT bundles was determined for the 7.5-nm technology node. The n-tier multilevel interconnect architecture for a 7.5-nm ASIC macrocell case study was designed using Cu and SWCNT bundle interconnects. It was shown that use of SWCNT bundles with $d = 1$ nm and $\beta = 1$ reduces the number of metal pairs and power dissipation by 27% and 25%, respectively, in comparison with Cu. It was also shown that decreasing AR of SWCNT bundle interconnects in multilevel interconnect design, decreases power dissipation by 41%. Impact of temperature variation on the n-tier interconnect architectures was studied and it was shown that higher pairs are more affected by temperature variation than lower pairs. Moreover, to mitigate temperature impact on interconnects performance, interconnect architectures can be designed for a higher temperature (350 K). Designing for a higher temperature, increases the number of metal pairs by 4.3%, but decreases dynamic power dissipation of repeaters by 0.6%.

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