Interconnect Scaling - The Real Limiter to High Performance ULSI

Mark T. Bohr

Portland Technology Development, Intel Corporation, Hillsboro, OR, USA 97124-6497

Abstract

Reducing interconnect pitch improves layout density, but degrades interconnect RC delay. Increasing metal aspect ratio (thickness/width) improves RC delay, but maximum benefits are achieved at an aspect ratio of ~2. Adding more interconnect layers improves density and performance, but practical limits are reached in just a few generations. New conductor and dielectric materials and improved circuit design techniques will be needed to meet future ULSI interconnect requirements.

Introduction

Consistent improvements in integrated circuit density and performance have been amply demonstrated over the past 20 years by using transistor scaling, a model for simultaneously improving transistor density and performance [1]. Fig. 1 shows how transistor performance will continue to improve proportional to feature size down to at least the 0.1 µm generation [2]. While transistor scaling continues to be necessary, metal interconnects are now a significant limiter and are as important as transistors in determining ULSI density and performance. Fig. 2 illustrates how simulated interconnect delay degrades with feature size reduction. Each technology generation represents a 0.7x reduction in feature size and interconnect delay degrades at a rate of 2x per generation assuming a constant metal aspect ratio and no change in conductor or dielectric materials. Interconnect delay for large high frequency chips is already a significant portion of the clock cycle time and will soon exceed the cycle time requirements if traditional interconnect scaling is continued.

Interconnect Trends and Options

Fig. 3 and 4 show how interconnects have scaled on the last five generations of Intel logic technology. The average metal pitch (P_{avg}) is defined as the sum of the minimum pitch used for each layer divided by the number of metal layers. P_{avg} has reduced by 0.77x per generation, while the number of metal layers has increased at a rate of 0.75 layers per generation. The average metal thickness has remained constant, resulting in average metal aspect ratios increasing from 0.4 to 1.3. Up to this point in time, increases in aspect ratio have been limited by the ability to pattern and etch metal spaces and the ability to fill them with an inter-level dielectric.

A simple first-order model can be used to estimate interconnect RC delay using the cross-section shown in Fig. 5. Assuming that the minimum metal pitch (P) equals twice the metal width (W), and assuming that the dielectric thickness above and below a metal line equals the thickness of the metal line, and using L to denote line length, the following equations can be used to estimate line resistance (R), line capacitance (C) and RC delay:

$$R = 2\rho L/PT \qquad (1)$$

$$C = 2(C_L + C_V) = 2\varepsilon\varepsilon_0(2LT/P + LP/2T) \qquad (2)$$

$$RC = 2\rho\varepsilon\varepsilon_0(4L^2/P^2 + L^2/T^2) \qquad (3)$$

As shown in Fig. 6, the relative RC delay of an interconnect of constant length has increased by 1.26x per generation. This is better than the trend shown in Fig. 2 because Fig. 2 assumes a constant metal aspect ratio, while on Intel technologies, the trend has been to increase aspect ratio. Continuing to increase aspect ratio on future technology generations will not bring similar benefits because the reduction in metal resistance will be offset by an increase in lateral capacitance (C_L). Using equation (3), interconnect RC delay can be calculated as a function of metal thickness and aspect ratio. As shown in Fig. 9, the RC delay benefits from increasing aspect ratio diminish above aspect ratios of ~2.

Reducing the dielectric constant of the inter-level dielectric will improve interconnect delay and reduce AC power consumption. Many low-ε dielectrics are being investigated, including fluorine-doped SiO_2, polymers and aerogels, with the best providing almost a factor of 2 reduction in ε [3, 4]. Many challenges remain, however, in identifying a low-ε material that also has the mechanical and reliability properties required in integrated circuits. Such properties include good adhesion between metal and dielectric layers, stability under high temperature processing and the ability to fill narrow spaces between metal lines. The interconnect delay benefit of reducing ε from 4 to 2 is illustrated in Fig. 9.

0-7803-2700-4 $4.00 ©1995 IEEE

Copper is an attractive substitute for standard aluminum interconnects due to its lower resistivity and improved electromigration resistance. The resistivity of pure Cu is 1.7 μΩ-cm compared to 3.0 μΩ-cm for Al-0.5%Cu alloys typically used in the industry today. Cu interconnects have also demonstrated electromigration resistance on the order of 10x better than Al interconnects [5]. A resistivity comparison between Cu and Al also needs to comprehend the relatively high resistance shunt and barrier layers incorporated in the metal stacks which detract from the net conductivity of a given metal cross-section (see Fig. 7). In the case of Al, a shunt layer consisting of Ti, TiN or TiW is used to improve electromigration resistance. In the case of Cu, a damascene structure is needed to form the interconnects because of difficulties with plasma etching Cu [6, 7]. With damascene, a thin barrier layer coats three sides of the conductor. This barrier layer usually consists of TiN, Ta or W and can significantly detract from net conductivity as line widths decrease. A barrier layer is needed with Cu to provide adhesion and to prevent Cu from diffusing through the inter-level dieletric and causing line-line leakage as shown in Fig. 8 [8]. The benefits of Cu on interconnect delay and the effects of shunt and barrier layer thicknesses are shown in Fig. 9. Although the barrier layer for Cu was thinner than the shunt layer for Al in this example (0.04 vs. 0.10 μm), the Cu barrier layer had a larger percentage impact on interconnect delay because it forms on three sides of the conductor. Considerable work remains before Cu can be successfully implemented in high volume manufacturing and the key process challenges include formation of thin barrier layers effective at containing Cu and deposition of high quality Cu films in high aspect ratio trenches.

Interconnect Scaling Requirements

Equation (3) offers a performance metric for interconnects, but a density metric that comprehends both interconnect pitch and number of layers is also needed to fully understand future interconnect scaling requirements. A proposed density metric is effective metal pitch (P_{eff}) which is defined as P_{avg} divided by the number of metal layers (N):

$$P_{eff} = P_{avg}/N \qquad (4)$$

Using equations (3) and (4), P_{avg} and N for future technology generations can be calculated given certain density (P_{eff}) and performance (RC) goals. P_{eff} should scale at the same rate as other minimum dimensions, typically 0.7x per generation. A metal aspect ratio of 2 is assumed to be a practical upper limit, therefore T = P in equation (3). Line length will be assumed to be constant. Figure 10 shows P_{avg} trends for three different interconnect performance goals. Without any material changes, P_{avg} will have to increase to realize any improvements in RC delay. Density goals (P_{eff}) must then be realized by increasing the number of metal layers, but an impractical number of metal layers is reached in only 1-3 generations with this approach, depending on what RC delay goal is set (Fig. 11). Reducing dielectric constant and/or metal resistivity helps to reduce the number of metal layers, but an impractical number is still reached in 3-4 generations, assuming RC delay is held constant at 1.0x per generation (Fig. 12). A more aggressive RC delay improvement goal would lead to an even more rapid increase in the number of metal layers. This analysis highlights the critical importance of developing improved interconnects to maintain ULSI density and performance trends. Interconnect material changes such as Cu and low-ε dielectrics will help considerably, but other innovations will be needed as well. Circuit design needs to more accurately model interconnect performance to avoid overdesign or unexpected performance limitations, and automatic layout tools need to make more efficient use of existing interconnects.

Conclusion

The trend of increasing interconnect RC delay with reductions in interconnect pitch will not support the performance requirements of future ULSI circuits. Increasing metal aspect ratios and adding more layers of interconnect are two techniques for improving interconnect performance and density, but these approaches will reach practical limits in just a few generations. New interconnect materials as well as improved circuit design techniques will be needed to address the growing limitation that interconnects pose to ULSI performance.

References

[1] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, A.R. LeBlanc, *IEEE J. Solid-State Circuits*, SC-9 (1974) p. 256.

[2] M.T. Bohr, *Semiconductor International*, Vol. 18, No. 6 (1995) p. 75.

[3] R.K. Laxman, *Semiconductor International*, Vol. 18, No. 5 (1995) p. 71.

[4] J. Paraszczak, D. Edelstein, S. Cohen, E. Babich, J. Hummel, *Intl. Electron Devices Meeting Tech. Digest* (1993) p. 261.

[5] T. Takewaki, T. Ohmi, T. Nitta, *Symposium on VLSI Technology, Digest of Tech. Papers* (1995) p. 31.

[6] A.V. Gelatos, S. Poon, R. Marsh, C.J. Mogab, M. Thompson, *Intl. Electron Devices Meeting Tech. Digest* (1994) p. 123.

[7] J. Li, T.E. Seidel, J.W. Mayer, *MRS Bulletin*, Vol XIX, No. 8 (1994) p. 15.

[8] G. Raghavan, C. Chiang, P.B. Anders, S.M. Tzeng, R. Villasol, G. Bai, M. Bohr, D.B. Fraser, *Thin Solid Films*, Vol. 262, Nos. 1-2, (1995) p. 168.

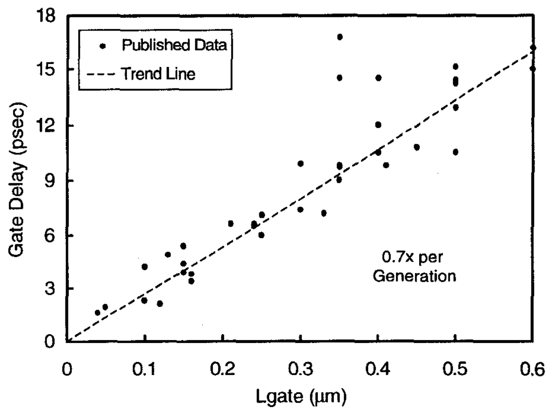

Fig. 1 N-ch MOSFET CV/I gate delay vs. physical gate length

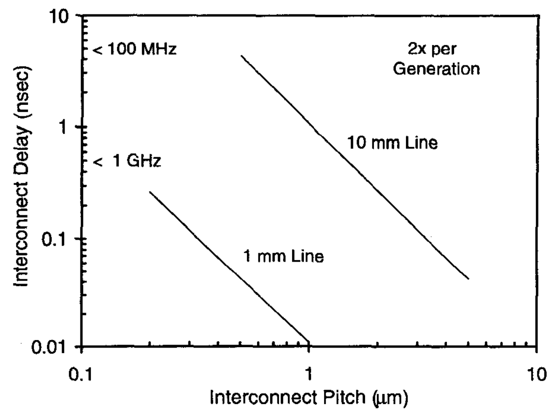

Fig. 2 Interconnect delay vs. line length and pitch (aspect ratio held constant at 2)

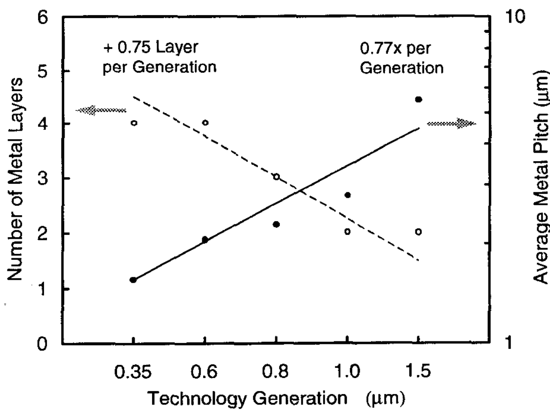

Fig. 3 Average minimum metal pitch and number of metal layers for Intel logic technologies

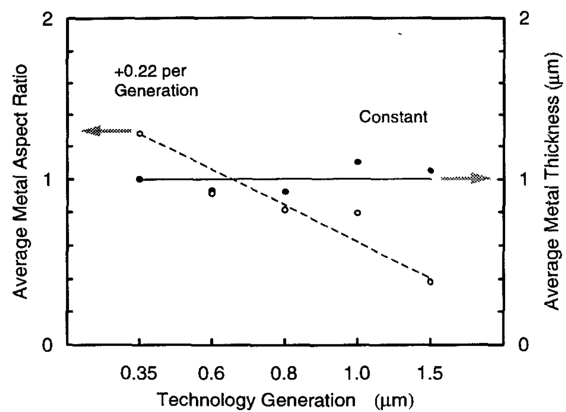

Fig. 4 Average metal thickness and aspect ratio for Intel logic technologies

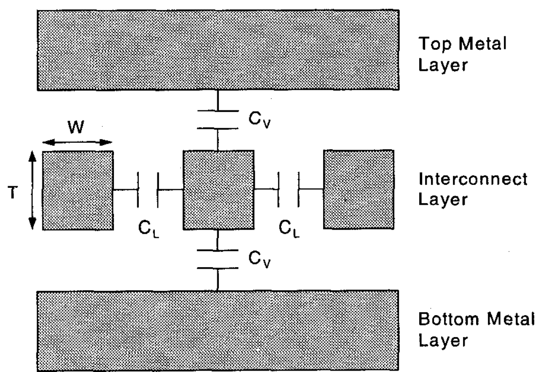

Fig. 5 Interconnect system cross-section with parasitic capacitances

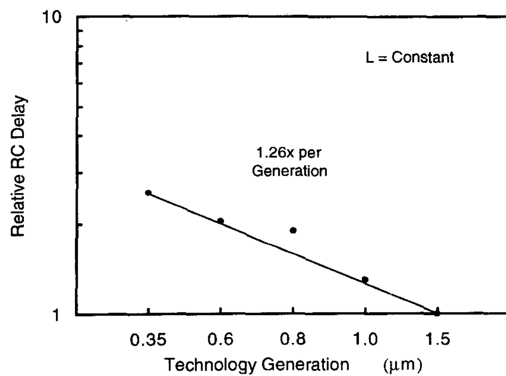

Fig. 6 Relative interconnect RC delay for Intel logic technologies

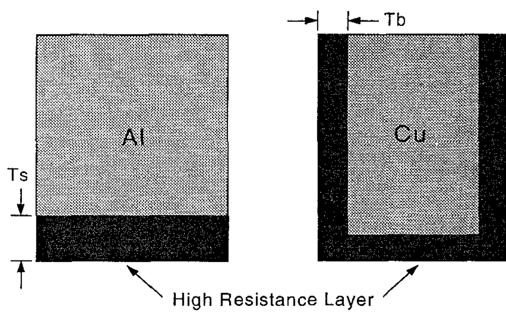

Fig. 7a Al Interconnect Fig. 7b Cu Interconnect

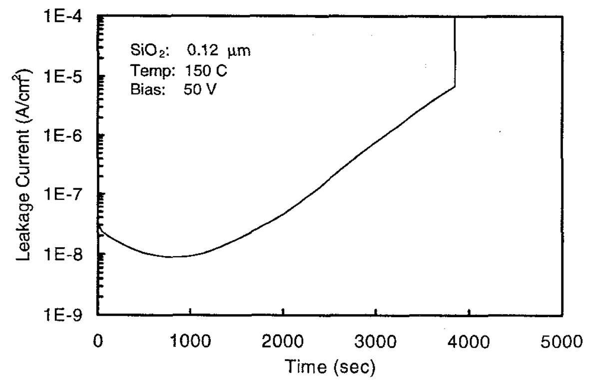

Fig. 7 Interconnect cross-sections showing impact of high resistance shunt or barrier layers

Fig. 8 Dielectric leakage due to Cu diffusion under bias and temperature stress

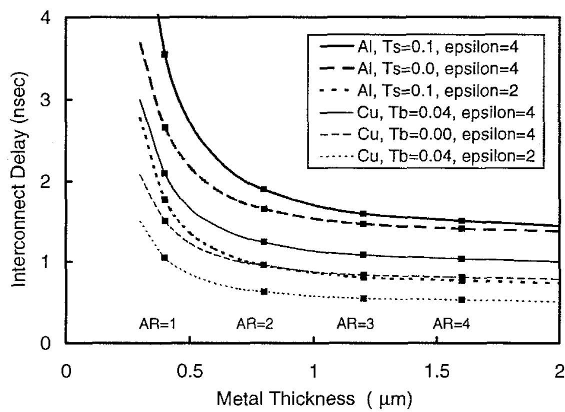

Fig. 9 Interconnect RC delay vs. thickness and material for 0.8 µm pitch and 10 mm length

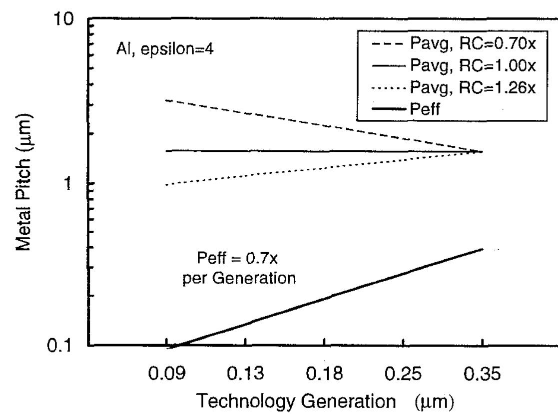

Fig. 10 Metal pitch trend vs. RC delay goal for standard Al interconnects

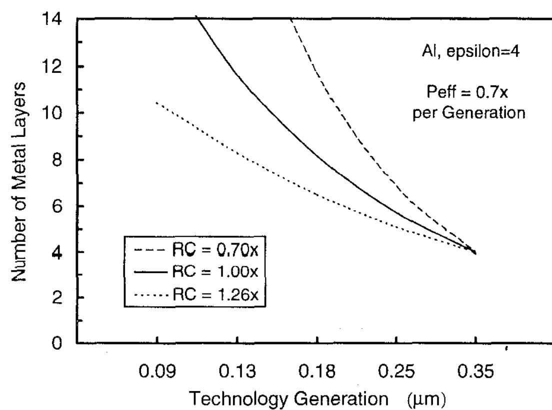

Fig. 11 Number of metal layers trend vs. RC delay goal for standard Al interconnects

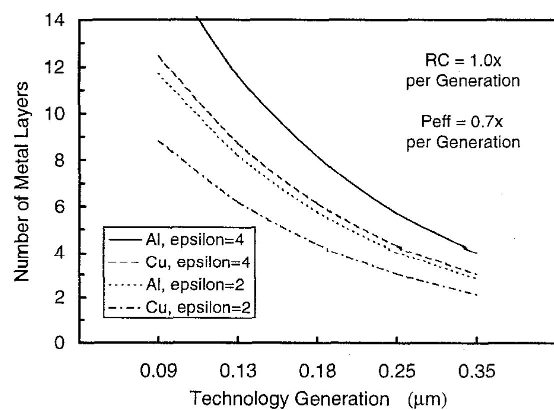

Fig. 12 Number of metal layers trend vs. interconnect material for an RC delay goal of 1.0x