A Stochastic Wire-Length Distribution for Gigascale Integration (GSI)—Part I: Derivation and Validation

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(Invited Paper)

***Abstract*—Based on Rent's Rule, a well-established empirical relationship, a rigorous derivation of a complete wire-length distribution for on-chip random logic networks is performed. This distribution is compared to actual wire-length distributions for modern microprocessors, and a methodology to calculate the wire-length distribution for future gigascale integration (GSI) products is proposed.**

***Index Terms*—Interconnect density function, interconnect projections, Rent's Rule, stochastic system modeling, wire-length distribution.**

I. Introduction

CLOCK frequency, power consumption, and chip size are largely determined by the wiring requirements of a VLSI system [1]–[3]. It is, therefore, imperative to gain thorough understanding of wiring requirements for present and projected gigascale integrated systems. To enhance this understanding, a new wire-length distribution is rigorously derived to enable first-order estimation of the wiring requirements for gigascale integration (GSI). Unlike previous distributions that describe only local interconnect requirements [4], [5], the new distribution provides a complete description of local, semi-global, and global wiring requirements.

In Section II, the assumptions and derivation of the new wire-length distribution are rigorously examined. In Section III, the new wire-length distribution is compared to data from real systems, and a methodology for calculating the wire-length distribution for future generation products is discussed. A companion paper [6] investigates various applications of the wire-length distribution such as determination of a critical path model, a dynamic power dissipation model, and an optimal multilevel wiring architecture for GSI.

II. Derivation of Wire-Length Distribution

A. Assumptions

Some early work on wiring distributions, especially [10], assumed that the wires emanating from a logic block follow a Poisson distribution. The primary assumption of this wire-length distribution model, however, is based upon a well-established empirical relationship commonly known as Rent's Rule [2], [7]–[9]. This relationship correlates the number of signal input and output (I/O) terminals T, to the number of gates N, in a random logic network. This correlation is given by a simple power law expression [2], [7]–[8]

$$T = kN^p \tag{1}$$

where the parameters k and p are empirical constants.

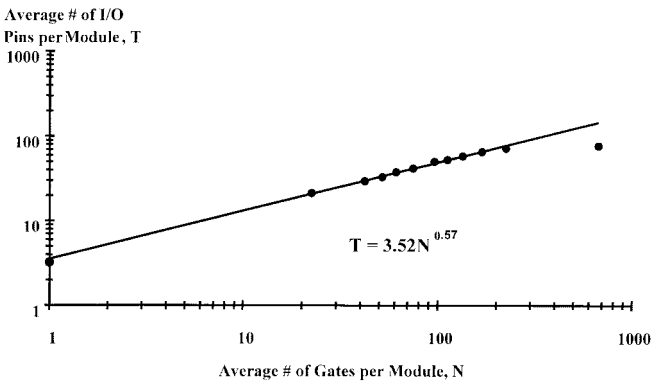

Fig. 1. Landman and Russo correlation between the number of module I/O terminals and the number of gates per module, after [7].

Early compelling evidence of Rent's Rule comes from a study by Landman and Russo [7], who partitioned existing scientific computers into modules and discovered an average relationship between the number of gates in a module and the number of module I/O terminals, as illustrated in Fig. 1. More recently, Bakoglu examined a variety of microprocessor, ASIC, memory, and gate array chips, and found that similar power law relationships describe the external I/O requirements of these systems, as seen in Fig. 2 [2]. In addition, the external I/O pins for the Intel microprocessor family, from the Intel 4004 in 1971 up to the Pentium Pro in 1996, are estimated by Rent's Rule, as shown in Fig. 3.

The underlying assumption of this derivation is based upon the recursive application of Rent's Rule throughout an entire monolithic system. As seen in Fig. 4, for any arbitrary closed path within a system of N gates, Rent's Rule determines the I/O requirements of the enclosed collections of gates.

B. The Complete Wire-Length Distribution

To predict the interconnect requirements for future GSI products, a continuous interconnect density function, i.d.f., is defined such that the number of interconnects between length

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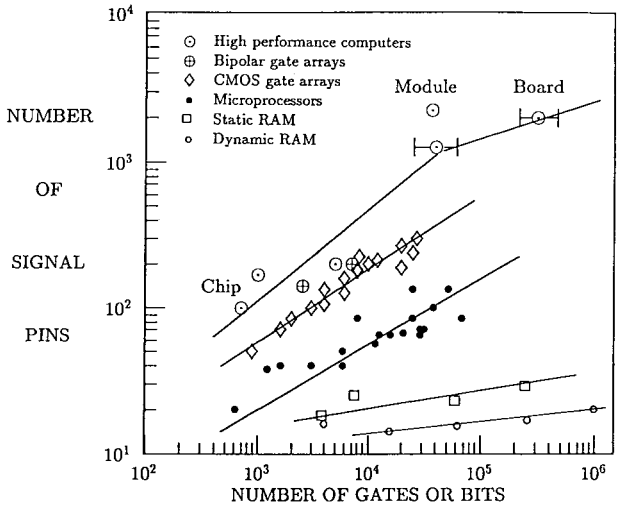

Fig. 2. Bakoglu correlation between the number of external chip terminals (signal pins) and the number of gates, after [2].

$\ell = a$ and $\ell = b$ is

$$I(a < \ell < b) = \int_a^b i(\ell)\, d\ell. \tag{2}$$

From Appendixes A, B, and C, the closed form expression for the i.d.f. for a square array of homogeneous logic gates is

Region I: $1 \le \ell \le \sqrt{N}$

$$i(\ell) = \frac{\alpha k}{2}\,\Gamma\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right)\ell^{2p-4}$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$i(\ell) = \frac{\alpha k}{6}\,\Gamma(2\sqrt{N} - \ell)^3\ell^{2p-4} \tag{3}$$

where ℓ is the interconnect length in units of gate pitches, N is the number of logic gates, p is Rent's exponent, α is the fraction of the on-chip terminals that are sink terminals and is related to average fanout, f.o., as

$$\alpha = \frac{\text{f.o.}}{\text{f.o.} + 1} \tag{4}$$

and Γ is

$$\Gamma = \frac{2N(1 - N^{p-1})}{\left(-N^p\,\dfrac{1 + 2p - 2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \dfrac{1}{6p} + \dfrac{2\sqrt{N}}{2p-1} - \dfrac{N}{p-1}\right)}. \tag{5}$$

At $p = 0.5, \Gamma$ is an indeterminate of the form 0/0, but using L' Hospital's rule at $p = 0.5$ the normalization factor Γ, converges to

$$\Gamma = \frac{4N - 4\sqrt{N}}{\sqrt{N}(-2.0\ln N - 6.0 + 2.0\ln 4) + 4.0N - \dfrac{2}{3}}. \tag{6}$$

Furthermore, the cumulative interconnect distribution function, c.i.d.f., gives the total number of interconnects that have a length less than and equal to ℓ

$$I(\ell) = \int_1^\ell i(\zeta)\, d\zeta \tag{7}$$

where ζ is a variable of integration and ℓ is the length of the interconnect in gate pitches. Evaluating (7) gives the expression for the c.i.d.f. $I(\ell)$

Region I: $I \le \ell < \sqrt{N}$

$$I(\ell) = \frac{\alpha k}{2}\,\Gamma\left(\frac{\ell^{2p} - 1}{6p} + 2\sqrt{N}\,\frac{-\ell^{2p-1} + 1}{(2p-1)} - N\,\frac{-\ell^{2p-2} + 1}{(p-1)}\right)$$

Region II: $\sqrt{N} \le \ell \le 2\sqrt{N}$

(see (8) at the bottom of the page). The compact closed form analytical expressions for the i.d.f. and the c.i.d.f. in (3) and (8) are compared to computer simulation of the exact interconnect distribution derived in Appendix A in (A16).

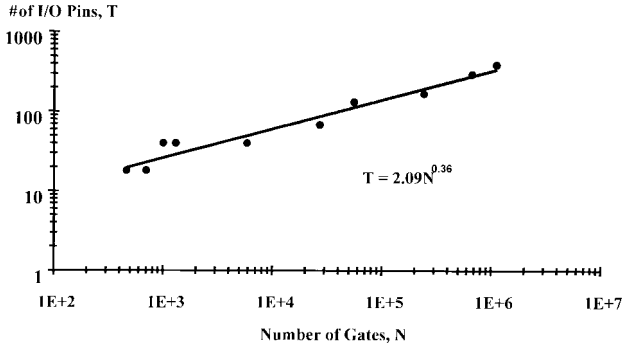

Fig. 3. Number of external chip terminals (signal pins) versus number of gates for the Intel microprocessor family.

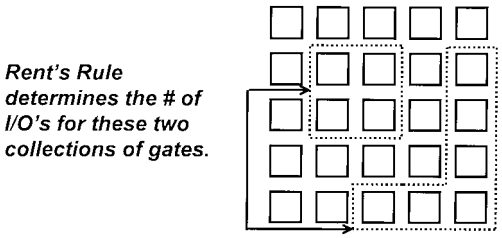

Fig. 4. Critical assumption of the wire-length distribution.

$$I(\ell) = \frac{\alpha k}{2}\,\Gamma\left(\begin{array}{l}\dfrac{N^{2p} - 1}{6p} + 2\sqrt{N}\,\dfrac{-N^{2p-1} + 1}{2p-1} - N\,\dfrac{-N^{2p-2} + 1}{(p-1)} \\ +\dfrac{1}{3}\left(-8N^{3/2}\,\dfrac{-\ell^{2p-3} + N^{p-(3/2)}}{(2p-3)} + 6N\,\dfrac{-\ell^{2p-2} + N^{p-1}}{(p-1)}\right. \\ \left. -6\sqrt{N}\,\dfrac{-\ell^{2p-1} + N^{p-(1/2)}}{(2p-1)} + \dfrac{-\ell^{2p} + N^p}{2p}\right)\end{array}\right). \tag{8}$$

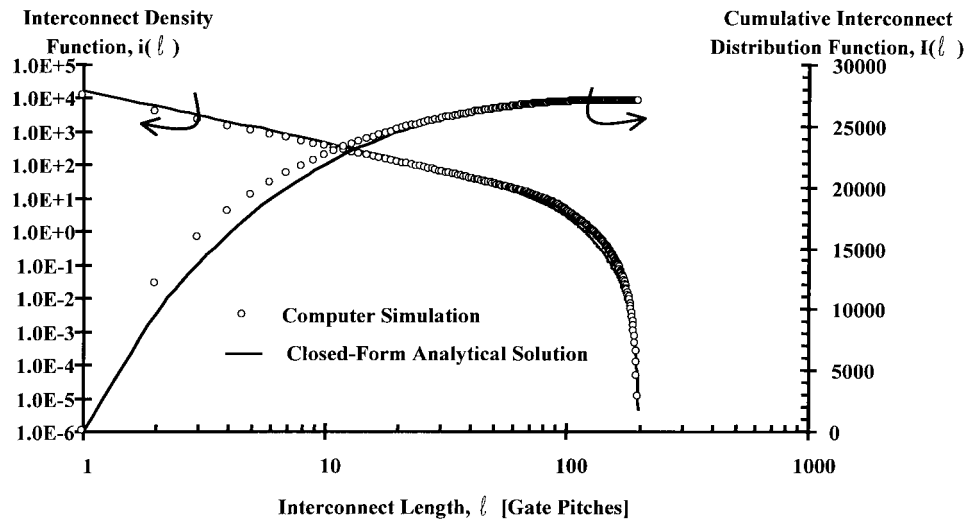

Fig. 5. Computer simulation compared to closed-form expressions for a system with $N = 1e4,\ p = 0.75,\ k = 4.0$, average fanout = 3.0.

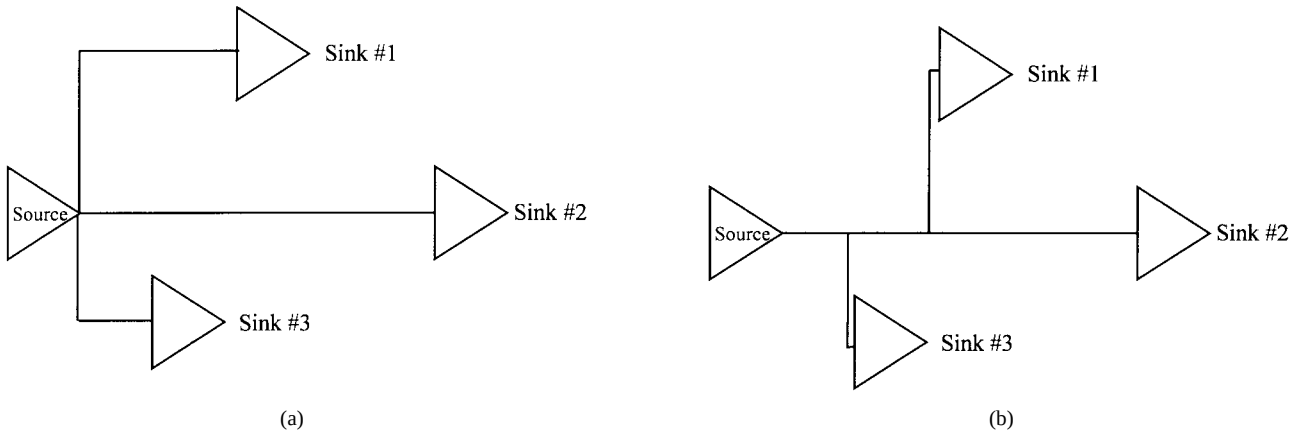

Fig. 6. Schematic of (a) a point-to-point interconnect and (b) a real wiring net.

C. Net Model Extension

In real random logic networks, the source terminals (i.e., the output I/O's) are usually connected to multiple sink terminals (i.e., the input I/O's). The i.d.f. predicts the number of point-to-point interconnects connecting a source terminal to each of its sink terminals, as seen in Fig. 6(a). Real designs, however, use wiring "nets" that more efficiently connect the source to its sink terminals as illustrated in Fig. 6(b) [2].

The more efficient wiring nets must be considered when estimating total wiring area, total wiring capacitance, and wiring net performance [2]. In order to estimate these physical quantities, a regular linear net model is used to approximate the geometrical layout of a real wiring net. The geometrical configuration of this net model is seen in Fig. 7, where each subsection of the net is assumed to have equal lengths s.

Given a f.o., the cumulative length of the point-to-point interconnects L_{point} for one linear wiring net is

$$L_{\text{point}} = 2s + 3s \cdots (\text{f.o.} + 1)s = \sum_{k=1}^{\text{f.o.}} (k+1)s = s\left(\frac{\text{f.o.}}{2}(\text{f.o.} + 3)\right). \tag{9}$$

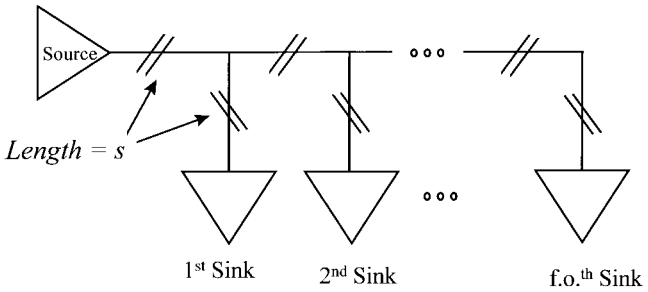

Fig. 7. Linear wiring net model.

The length of each segment s is

$$s = \frac{L_{\text{net}}}{2(\text{f.o.})} \tag{10}$$

where L_{net} is the net length for a single wiring net with a given f.o.

Therefore, the net length in terms of the cumulative length of the point-to-point interconnects L_{point} for the linear net model is

$$L_{\text{net}} = \chi L_{\text{point}} \tag{11}$$

where $\chi = 4/\text{f.o.} + 3$.

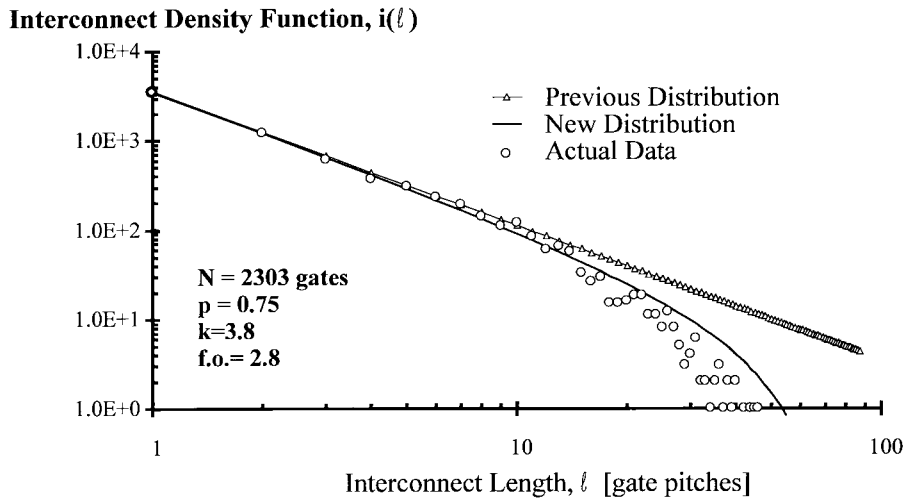

Fig. 8. Comparison of the new stochastic model to actual data and a previous stochastic model.

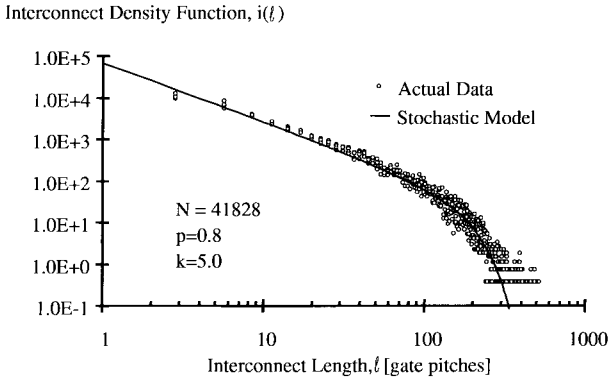

Fig. 9. Interconnect density function compared to the interconnect histogram for microprocessor A.

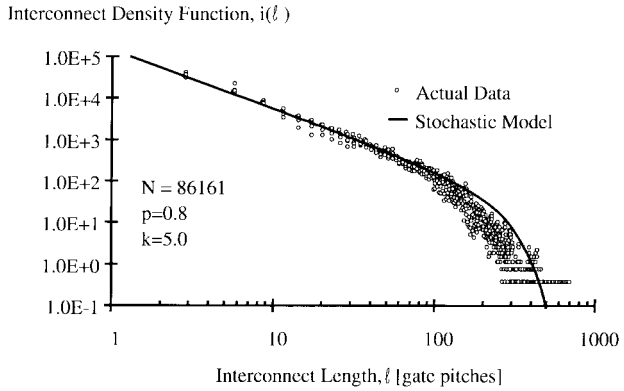

Fig. 10. Interconnect density function compared to the interconnect histogram for microprocessor B.

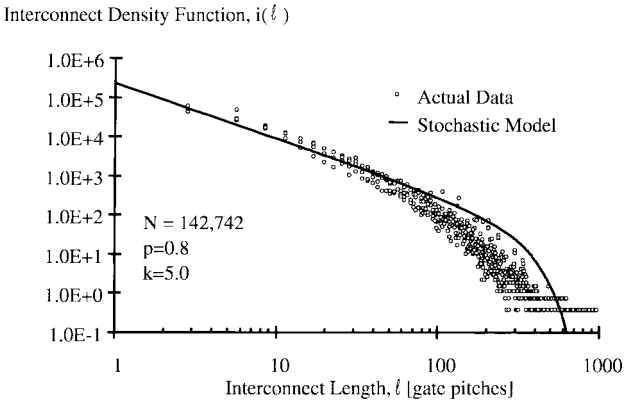

Fig. 11. Interconnect density function compared to the interconnect histogram for microprocessor C.

III. Comparisons with Actual Data

The new i.d.f. characterizes real data with high accuracy. In Fig. 8 it is compared to actual point-to-point interconnect data taken from a real system [4] and also to a widely cited previous wire-length distribution model [4]. As seen in Fig. 8, the complete i.d.f. describes a real wiring histogram with higher fidelity than previous models [4], [5].

Moreover, comparisons to current data on microprocessors indicate that the new i.d.f. accurately estimates the wiring for these VLSI systems. Fig. 9 contains a wiring distribution for a current microprocessor design. The uncertainty in the actual data is due to different wiring net models that were used to convert the net list information for this microprocessor to point-to-point wiring information. The specifications of these net models are contained in Appendix C. The k and p empirical parameters were chosen to obtain a best fit of the data for microprocessor A in Fig. 9.

Using the k and p parameters derived from microprocessor A, the i.d.f. is now used to predict the i.d.f. for subsequent generations of microprocessors from the same company as seen in Figs. 10 and 11. The i.d.f. provides a good first-order estimation of the wiring requirements of microprocessors B and C.

Determination of the best values of k and p parameters for future generation products mandates an investigation into previous generations of a product family. As shown with microprocessors A, B, and C, the heredity of a particular product generation usually has a strong influence on its k and p values. This also is particularly striking for the Intel microprocessor family, as illustrated in Fig. 3.

IV. Conclusion

Based upon Rent's Rule, a new complete stochastic wiring distribution is rigorously derived that determines wire-length

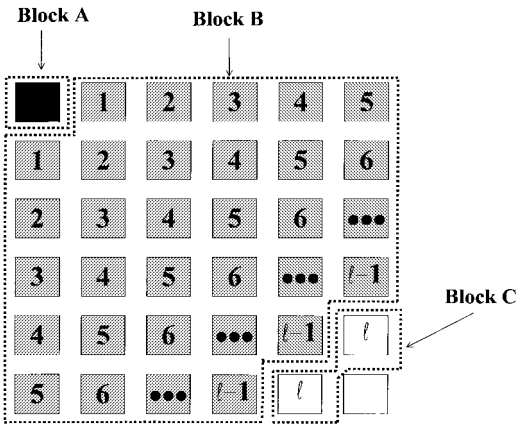

Fig. 12. Determination of wire-length distribution for a single gate.

frequency for a homogeneous array of random logic gates, and it enables a priori estimation of the wiring requirements for future GSI systems. Unlike previous distributions that describe only local interconnect requirements [4], [5], the new distribution provides a complete description of local, semi-global, and global wiring requirements. The new wire-length distribution is verified through comparisons to actual data from real systems, and a methodology to calculate the wire-length distribution for future GSI products is proposed.

APPENDIX A
DERIVATION OF POINT-TO-POINT WIRING DISTRIBUTION

Before the complete wire-length distribution for an entire monolithic system is derived, the stochastic wire-length distribution of a single gate must be calculated. To illustrate this calculation for a single gate without loss of generality, consider the corner element of a square array of gates as seen in Fig. 12. The expected number of interconnects from the corner element to all gates that are a distance ℓ away is determined using Rent's Rule.

The gates in Fig. 12 are grouped into three distinct but adjacent blocks, A, B, and C, such that a single closed path can encircle one, two, or all three of these blocks. The number of connections between Block A and Block C is calculated by conserving all I/O terminals for blocks A, B, and C. Conservation of I/O terminals states that the terminals for blocks A, B, and C are either inter-block connections or external system connections.

For instance, applying the principle of conservation of I/O's to the three block system in Fig. 12 gives

$$T_A+T_B+T_C=T_{A\text{-to-}C}+T_{A\text{-to-}B}+T_{B\text{-to-}C}+T_{ABC} \quad \text{(A1)}$$

where these variables are defined in Table I.

Because blocks A and B are adjacent, one closed curve is drawn to encircle A and B. From conservation of terminals, the number of I/O's between blocks A and B is written as

$$T_{A\text{-to-}B}=T_A+T_B-T_{AB}. \quad \text{(A2)}$$

Likewise, because blocks B and C are adjacent, the number of terminals between block B and C is written as

$$T_{B\text{-to-}C}=T_B+T_C-T_{BC}. \quad \text{(A3)}$$

TABLE I
VARIABLE DEFINITIONS

VARIABLE	DEFINITION
T_A	# of I/O's of block A
T_B	# of I/O's of block B
T_C	# of I/O's of block C
$T_{A\text{-to-}B}$	# of I/O's connecting block A to B
$T_{A\text{-to-}C}$	# of I/O's connecting block A to C
$T_{B\text{-to-}C}$	# of I/O's connecting block B to C
T_{AB}	# of I/O's of block A + B
T_{BC}	# of I/O's of block B + C
T_{ABC}	# of I/O's of block A+B+C

Substituting (A2) and (A3) into (A1) and simplifying gives

$$T_{A\text{-to-}C}=T_{AB}-T_B+T_{BC}-T_{ABC}. \quad \text{(A4)}$$

The number of I/O terminals for a single block is directly calculated from Rent's Rule. Assuming, N_A, N_B, and N_C are the number of gates in block A, block B, and block C, respectively, from (1) the number of terminals for each block is

$$T_B=k(N_B)^p \quad \text{(A5)}$$

$$T_{AB}=k(N_A+N_B)^p \quad \text{(A6)}$$

$$T_{BC}=k(N_B+N_C)^p \quad \text{(A7)}$$

$$T_{ABC}=k(N_A+N_B+N_C)^p. \quad \text{(A8)}$$

Substituting (A5)–(A8) into (A4) gives

$$T_{A\text{-to-}C}=k[(N_A+N_B)^p-(N_B)^p+(N_B+N_C)^p-(N_A+N_B+N_C)^p]. \quad \text{(A9)}$$

To calculate the number of interconnects between blocks A and C, define a variable α that is the fraction of terminals that are sinks (or input terminals) [9]. Therefore, the expected number of point-to-point interconnects between blocks A and C in Fig. 12 is

$$I_{A\text{-to-}C}=\alpha k[(N_A+N_B)^p-(N_B)^p+(N_B+N_C)^p-(N_A+N_B+N_C)^p]. \quad \text{(A10)}$$

The α factor is expressed in terms of the average fanout of the system, f.o., as

$$\alpha=\frac{\text{f.o.}}{\text{f.o.}+1}. \quad \text{(A11)}$$

Using (A10) to calculate the number of interconnects for each length ℓ in Fig. 12 in the range from one gate pitch to $2\sqrt{N}$ gate pitches, gives the complete stochastic wire-length distribution for the corner element. This is accomplished by tabulating the number of gates contained in N_A, N_B, and N_C for each length under consideration.

Once the stochastic wire-length distribution is determined for the corner element, it is "removed" from the system of gates for calculating the remainder of the wiring distribution in order to prevent multiple counting of interconnects. The same process is repeated for all other gates in the system. This algorithm is illustrated in Fig. 13. The wire-length distributions for individual gates are superimposed to obtain the wire-length distribution for the entire system of N gates.

To describe this algorithm mathematically, define a function $\Phi(i,j,\ell)$ that gives the number of gates that are a distance ℓ

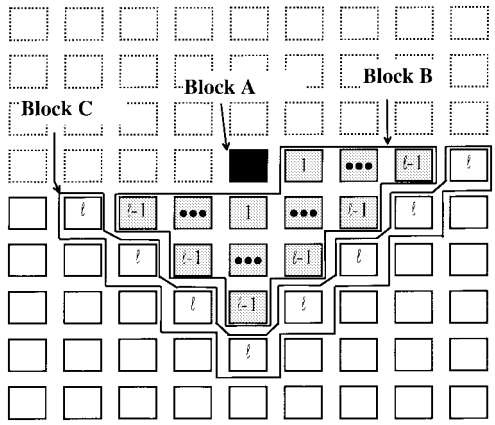

Fig. 13. Algorithm for exact wire-length distribution calculation.

away from the gate in the ith row and the jth column in a square array of gates, as seen in Fig. 13. This function excludes all gates that have been previously analyzed (i.e., the dashed gates in Fig. 13). Using step functions $u_o(x)$, the function $\Phi(i,j,\ell)$ is found from inspection to be (A12), shown at the bottom of the page.

Using $\Phi(i,j,\ell)$, N_A, N_B, and N_C are rigorously defined in general as

$$N_A = 1 \tag{A13}$$

$$N_B = \sum_{r=1}^{r=\ell-1} \Phi(i,j,r) \tag{A14}$$

$$N_C = \Phi(i,j,\ell). \tag{A15}$$

Using (A10) and (A13)–(A15) gives the exact formula for the discrete interconnect distribution

$$i(\ell) = \sum_{i=1}^{\sqrt{N}} \sum_{j=1}^{\sqrt{N}} \left[\left(1 + \sum_{r=1}^{l-1} \Phi(i,j,r) \right)^p - \left(\sum_{r=1}^{l-1} \Phi(i,j,r) \right)^p + \left(\sum_{r=1}^{\ell} \Phi(i,j,r) \right)^p - \left(1 + \sum_{r=1}^{\ell} \Phi(i,j,r) \right)^p \right]. \tag{A16}$$

Using (A16), computer simulation of this algorithm can be performed, but for a large number of gates, simulation time becomes excessive.

Appendix B
Closed Form Analytical Expression

The complete derivation of an exact wire-length distribution is presented in Appendix A. The final form of the exact wiring distribution appears in expression (A16). This expression is a double finite series summation that requires computer simulation to determine the final wiring distribution. In this appendix, a compact closed-form analytical approximation of the wiring distribution is derived.

To obtain a closed form analytical expression for the complete wire length that appears in (A16), it is assumed that on average the partitioning strategies are similar to the partial manhattan circle as seen in Fig. 13. From geometrical inspection, a partial manhatten circle with radius ℓ in a large square array of gates is the most common configuration for gates that are at a distance greater than ℓ from the chip perimeter.

The number of gates on the periphery of the partial manhattan circle is equal to twice the radius of the circle (2ℓ). Therefore, from Fig. 13 the expressions for N_A, N_B, and N_C are approximately given by

$$N_A = 1 \tag{B1}$$

$$N_B = \sum_{r=1}^{r=l-1} 2r = \ell(\ell-1) \tag{B2}$$

$$N_C = 2\ell \tag{B3}$$

where N_A, N_B, and N_C are the number of logic gates in block A, block B, and block C in Fig. 13.

Substituting (B1)–(B3) into (A10) gives the expected number of connections from the center gate of the partial manhattan circle (p.m.c) to all the periphery gates

$$I_{\text{p.m.c.}}(\ell) = \alpha k[(1+\ell(\ell-1))^p - (\ell(\ell-1))^p + (\ell(\ell+1))^p - (1+\ell(\ell+1))^p] \tag{B4}$$

where α is the fraction of I/O terminals that are sink terminals in (A11).

The average number of interconnects connecting each gate pair separated by a length ℓ in a given partial manhattan circle is obtained by dividing the number of interconnections given by (B4) by the number of gates on the periphery of a partial manhattan circle, 2ℓ. Using this partial manhattan circle approximation, the expected number of interconnects connecting gate pairs that are separated by a length ℓ in a given system is

$$I_{\exp}(\ell) = \frac{\alpha k}{2\ell} [(1+\ell(\ell-1))^p - (\ell(\ell-1))^p + (\ell(\ell+1))^p - (1+\ell(\ell+1))^p]. \tag{B5}$$

To complete the derivation for the entire wire-length distribution, the number of gate pairs $M(\ell)$ separated by a length ℓ in a square array of N gates must be determined. To begin the derivation of the number of gate pairs separated by a manhattan distance ℓ in a square array of N gates, first consider the function $\Phi(i,j,\ell)$ defined in (A12).

Summing $\Phi(i,j,\ell)$ over the entire $\sqrt{N}$ by $\sqrt{N}$ square array of gates gives $M(\ell)$, the total number of gate pairs separated

$$\Phi(i,j,\ell) = \begin{bmatrix} (\ell+1)u_o(\ell+1) - (\ell-\sqrt{N}+j)u_o(\ell-\sqrt{N}+j) \\ -(\ell-\sqrt{N}+i)u_o(\ell-\sqrt{N}+i) + (\ell-1)u_o(\ell-1) \\ +2(\ell-2\sqrt{N}+j+i-1)u_o(\ell-2\sqrt{N}+j+i-1) \\ -(\ell-\sqrt{N}-1+j)u_o(\ell-\sqrt{N}-1+j) \\ -(\ell-\sqrt{N}-1+i)u_o(\ell-\sqrt{N}-1+i) \end{bmatrix}. \tag{A12}$$

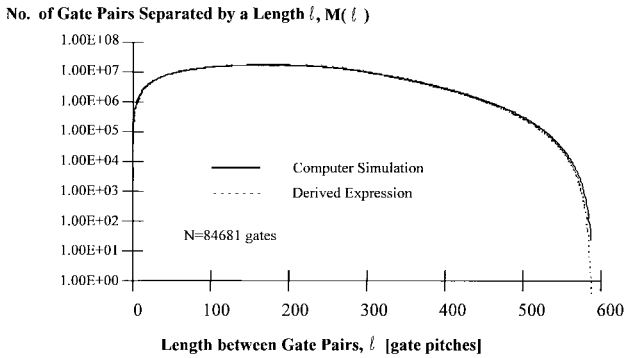

Fig. 14. Derived closed form expression versus exact computer calculation.

by a length ℓ

$$M(\ell) = \sum_{i=1}^{i=\sqrt{N}} \sum_{j=1}^{j=\sqrt{N}} \Phi(i,j,\ell). \tag{B6}$$

Evaluating (B6) exactly gives

Region I: $1 \le \ell < \sqrt{N}$

$$M(\ell) = \left(\frac{\ell^3}{3} - 2\ell^2\sqrt{N} + \frac{1}{3}\,\ell(6N-1)\right)$$

Region II: $\sqrt{N} \le \ell < (2\sqrt{N}-2)$

$$M(\ell) = \left(-\frac{\ell^3}{3} + 2\ell^2\sqrt{N} - \frac{1}{3}\,\ell(12N-1) + \frac{2}{3}\,\sqrt{N}(2\sqrt{N}-1)(2\sqrt{N}+1)\right). \tag{B7}$$

Assuming that $N \gg 1$, then (B7) simplifies to the final expression for the number of gate pairs separated by a length ℓ in a square array of N gates

Region I: $1 \le \ell < \sqrt{N}$

$$M(\ell) = \left(\frac{\ell^3}{3} - 2\ell^2\sqrt{N} + 2\ell N\right)$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$M(\ell) = \tfrac{1}{3}\,(2\sqrt{N}-\ell)^3. \tag{B8}$$

The closed form solution for $M(\ell)$ is checked against computer simulation in Fig. 14.

Therefore, the approximate expression for the discrete wirelength distribution $i'(\ell)$ that gives the expected number of interconnects for a given length ℓ is

$$i'(\ell) = M(\ell) I_{\exp}(\ell). \tag{B9}$$

$I_{\exp}(\ell)$ is simplified using a binomial expansion and is given by

$$I_{\exp}(\ell) \cong \alpha k\,\frac{p}{2}\,(2-2p) l^{2p-4}. \tag{B10}$$

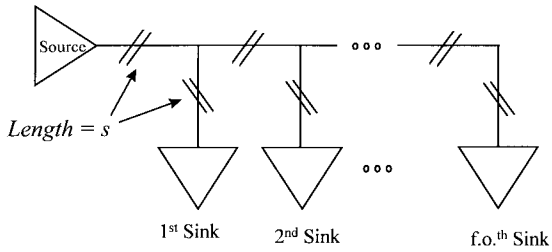

Fig. 15. Linear Net Model.

The final expression for the approximate un-normalized discrete interconnect distribution $i'(\ell)$ is given by

Region I: $1 \le \ell < \sqrt{N}$

$$i'(\ell) = \frac{\alpha k}{2}\,(2-2p)p\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right) l^{2p-4}$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$i'(\ell) = \frac{\alpha k}{6}\,(2-2p)p(2\sqrt{N}-\ell)^3 \ell^{2p-4} \tag{B11}$$

where ℓ is the interconnect length in units of gate pitches.

For a given k, p, α, and N, the total number of interconnects in a system from Rent's Rule is given by [9]

$$I_{\text{total}} = \alpha k N(1 - N^{p-1}). \tag{B12}$$

Using (B12), the discrete interconnect distribution is transformed to the discrete probability density function. The unnormalized probability density function $p'_{\text{int}}(\ell)$ is determined by dividing expression (B11) by (B12)

Region I: $1 \le \ell < \sqrt{N}$

$$p'_{\text{int}}(\ell) = \frac{(2-2p)p}{2N(1-N^{p-1})}\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right)\ell^{2p-4}$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$p'_{\text{int}}(\ell) = \frac{(2-2p)p}{6N(1-N^{p-1})}\,(2\sqrt{N}-\ell)^3 \ell^{2p-4}. \tag{B13}$$

The following expression is used to determine the normalized discrete probability density function:

$$1 = \Gamma' \sum_{I=1}^{2\sqrt{N}} p'_{\text{int}}. \tag{B14}$$

By making the assumption that $2\sqrt{N} \gg 1$, then the discrete distribution is approximated by a continuous probability density function (p.d.f.). The normalizing factor for the p.d.f. is determined from

$$\Gamma' = \frac{1}{\displaystyle\int_{\ell=1}^{2\sqrt{N}} p'_{\text{int}}(\ell)}. \tag{B15}$$

Evaluating (B15) gives (B16), shown at the bottom of the page.

$$\Gamma' = \frac{2N(1-N^{p-1})}{(2-2p)p\left(-N^p\,\dfrac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \dfrac{1}{6p} + \dfrac{2\sqrt{N}}{2p-1} - \dfrac{N}{p-1}\right)} \tag{B16}$$

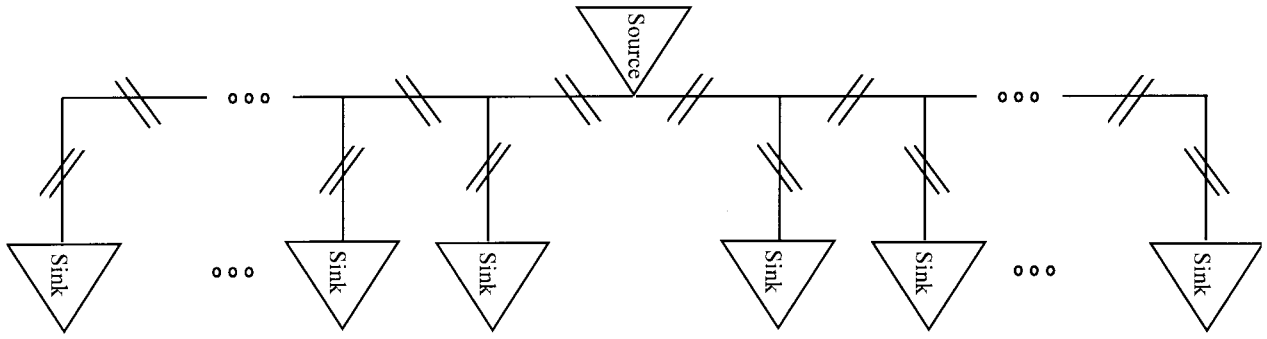

Fig. 16. Bi-directional Linear Net Model.

The expression for the normalized probability density function is $p_{\text{int}}(\ell) = \Gamma' p'_{\text{int}}(\ell)$. The full expression for $p_{\text{int}}(\ell)$ becomes

Region I: $1 \le \ell < \sqrt{N}$

$$p_{\text{int}}(\ell) = \frac{1}{2N(1-N^{p-1})}\Gamma\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right)\ell^{2p-4}$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$p_{\text{int}}(\ell) = \frac{1}{6N(1-N^{p-1})}\,\Gamma(2\sqrt{N}-\ell)^3\ell^{2p-4} \tag{B17}$$

where ℓ is the interconnect length in units of gate pitches, N is the number of gates, p is Rent's exponent, and the new unprimed Γ factor is (B18), shown at the bottom of the page. At $p = 0.5$, Γ is an indeterminate of the form 0/0, but using L'Hospital's rule at $p = 0.5$, Γ converges to

$$\Gamma = \frac{4N - 4\sqrt{N}}{\sqrt{N}(-2.0\ln N - 6.0 + 2.0\ln 4) + 4.0N - \dfrac{2}{3}}. \tag{B19}$$

The probability density function is defined such that the probability of having an interconnect between length $\ell = a$ and $\ell = b$ is

$$P(a < \ell < b) = \int_a^b p_{\text{int}}(\ell)\, d\ell. \tag{B20}$$

The cumulative distribution function, c.d.f. $P(\ell)$, gives the total probability that a given interconnect length is less than and equal to ℓ. This $P(\ell)$ is determined from the probability density function and is given by

$$P(\ell) = \int_1^\ell p(\zeta)\, d\zeta \tag{B21}$$

where ζ is a variable of integration and ℓ is the length of the interconnect in gate pitches. Evaluating (B19) gives the expression for the cumulative distribution function $P(\ell)$

Region I: $I \le \ell < \sqrt{N}$

$$P(\ell) = \frac{1}{2N(1-N^{p-1})}\,\Gamma\left(\frac{\ell^{2p}-1}{6p} + 2\sqrt{N}\frac{-\ell^{2p-1}+1}{(2p-1)} - N\,\frac{-\ell^{2p-2}+1}{(p-1)}\right)$$

Region II: $\sqrt{N} \le \ell \le 2\sqrt{N}$

(see (B22) at the bottom of the page).

Using the normalization factor Γ, the un-normalized discrete i.d.f. $i'(\ell)$, is transformed to the normalized continuous i.d.f. $i(\ell)$. The interconnect density function, i.d.f., is defined as

$$i(\ell) = I_{\text{total}} p_{\text{int}}(\ell). \tag{B23}$$

Substituting (B12) and (B17) gives

Region I: $1 \le \ell < \sqrt{N}$

$$i(\ell) = \frac{\alpha k}{2}\Gamma\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right)\ell^{2p-4}$$

Region II: $\sqrt{N} \le \ell < 2\sqrt{N}$

$$i(\ell) = \frac{\alpha k}{6}\,\Gamma(2\sqrt{N}-\ell)^3\ell^{2p-4}. \tag{B24}$$

$$\Gamma = \frac{2N(1-N^{p-1})}{\left(-N^p\,\dfrac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \dfrac{1}{6p} + \dfrac{2\sqrt{N}}{2p-1} - \dfrac{N}{p-1}\right)} \tag{B18}$$

$$P(\ell) = \frac{1}{2N(1-N^{p-1})}\,\Gamma\left(\begin{array}{l}\dfrac{N^{2p}-1}{6p} + 2\sqrt{N}\,\dfrac{-N^{2p-1}+1}{2p-1} - N\,\dfrac{-N^{2p-2}+1}{(p-1)} \\ +\dfrac{1}{3}\left(-8N^{3/2}\,\dfrac{-\ell^{2p-3}+N^{p-(3/2)}}{(2p-3)} + 6N\,\dfrac{-\ell^{2p-2}+N^{p-1}}{(p-1)}\right. \\ \left. -6\sqrt{N}\,\dfrac{-\ell^{2p-1}+N^{p-(1/2)}}{(2p-1)} + \dfrac{-\ell^{2p}+N^p}{2p}\right)\end{array}\right) \tag{B22}$$

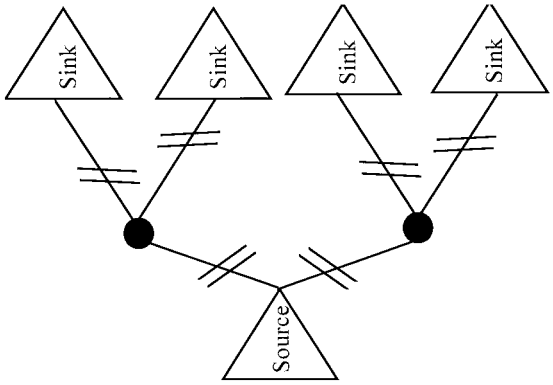

Fig. 17. Binary Tree Net Model #1 (all leaves are sinks).

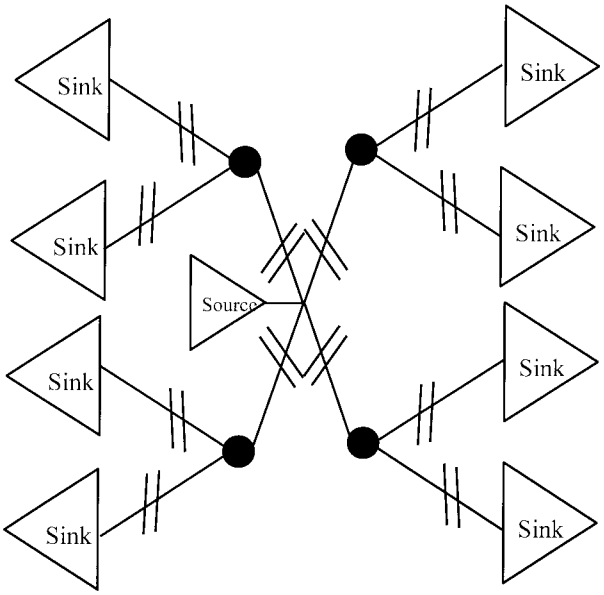

Fig. 18. Bi-directional Binary Tree Net Model #1 (all leaves are sinks).

The interconnect density function defined such that the number of interconnects between length $\ell = a$ and $\ell = b$ is

$$I(a < \ell < b) = \int_a^b i(\ell)\, d\ell. \tag{B25}$$

The cumulative interconnect distribution function, c.i.d.f., is determined from

$$I(\ell) = I_{\text{total}} P(\ell). \tag{B26}$$

Substituting (B12) and (B22) gives

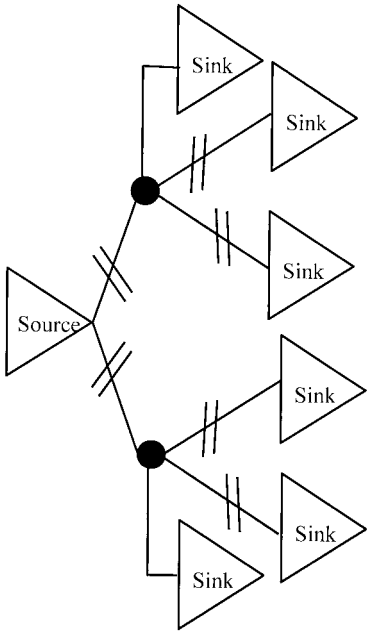

Fig. 19. Binary Tree Net Model #2 (all vertices are sinks).

Region I: $1 \le \ell < \sqrt{N}$

$$I(\ell) = \frac{\alpha k}{2}\,\Gamma\left(\frac{\ell^{2p}-1}{6p} + 2\sqrt{N}\frac{-\ell^{2p-1}+1}{(2p-1)} - N\,\frac{-\ell^{2p-2}+1}{(p-1)}\right)$$

Region II: $\sqrt{N} \le \ell \le 2\sqrt{N}$
(see (B27) at the bottom of the page).
The cumulative interconnect distribution function gives the total number of interconnects that have a length less than and equal to ℓ

$$I(\ell) = \int_1^{\ell} i(\zeta)\, d\zeta. \tag{B28}$$

The closed form analytical expressions for the i.d.f. and the c.i.d.f. are compared to computer simulation of expression (A16) in Fig. 5.

Appendix C
Catalog of Wiring Network Models

Several regular wiring net models are used to extract the point to point interconnect information given a net list of a

$$I(\ell) = \frac{\alpha k}{2}\,\Gamma\left(\begin{array}{l} \dfrac{N^{2p}-1}{6p} + 2\sqrt{N}\,\dfrac{-N^{2p-1}+1}{2p-1} - N\,\dfrac{-N^{2p-2}+1}{(p-1)} \\ +\dfrac{1}{3}\left(-8N^{3/2}\,\dfrac{-\ell^{2p-3}+N^{p-(3/2)}}{(2p-3)} + 6N\,\dfrac{-\ell^{2p-2}+N^{p-1}}{(p-1)}\right. \\ \left. -6\sqrt{N}\,\dfrac{-\ell^{2p-1}+N^{p-(1/2)}}{(2p-1)} + \dfrac{-\ell^{2p}+N^{p}}{2p}\right) \end{array}\right) \tag{B27}$$

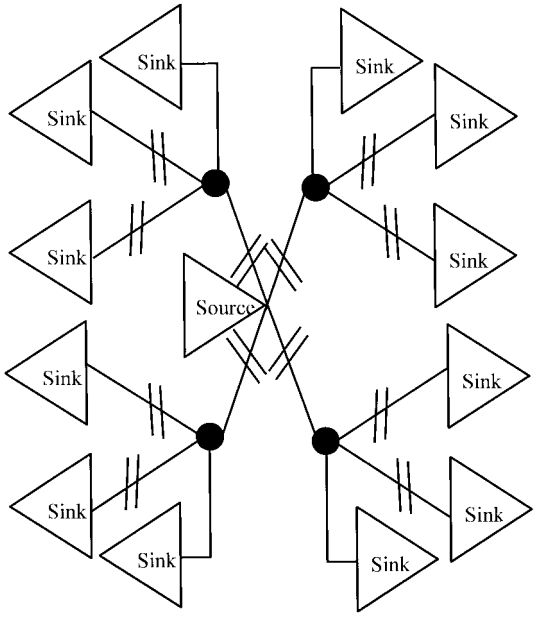

Fig. 20. Bi-directional Binary Tree Net Model #2 (all vertices are sinks).

real system. The schematics of these wiring net models are illustrated in Figs. 15–20.

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