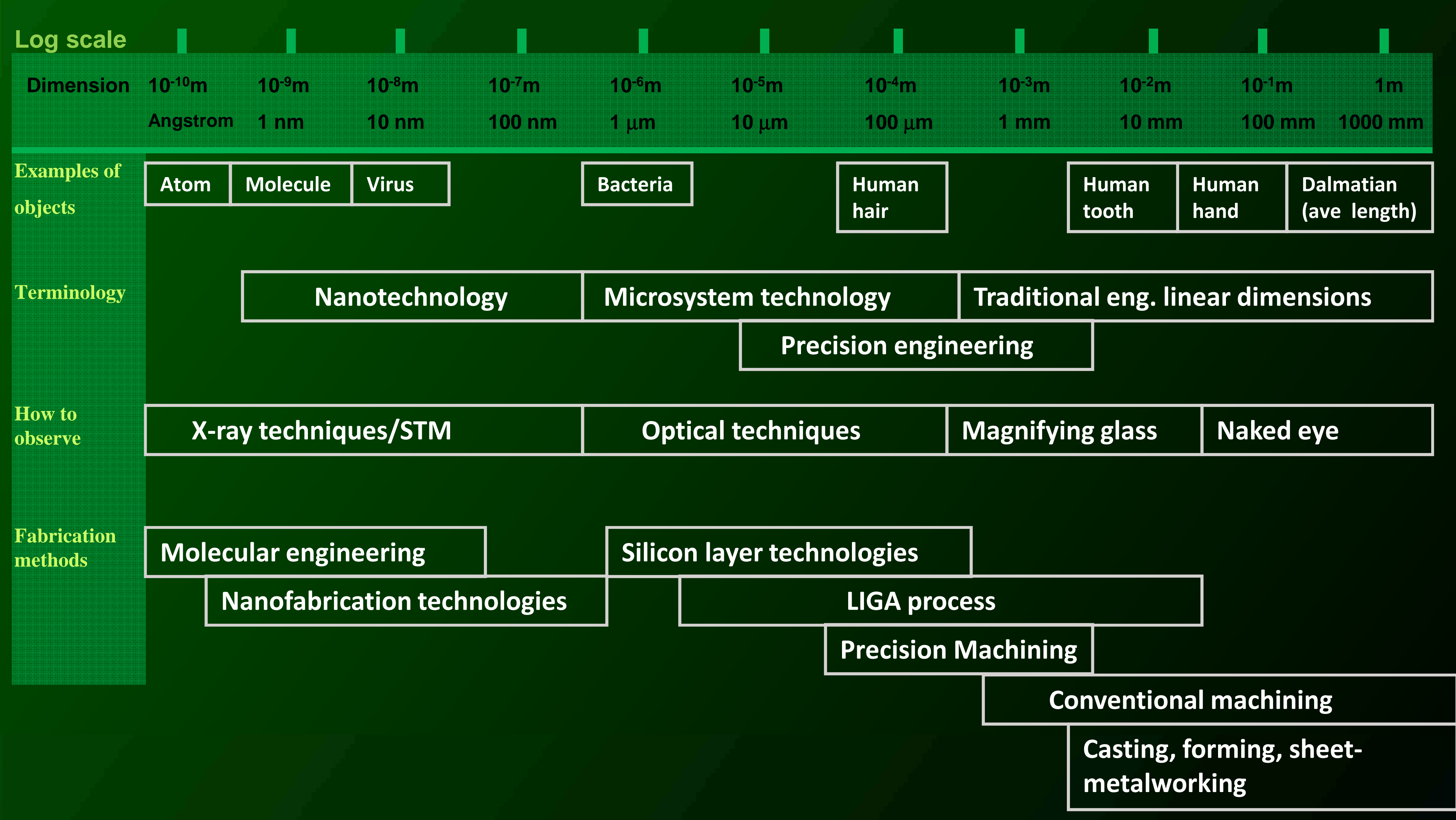
Session 1: Lithography

Nano Technology

Terminology and Relative Sizes

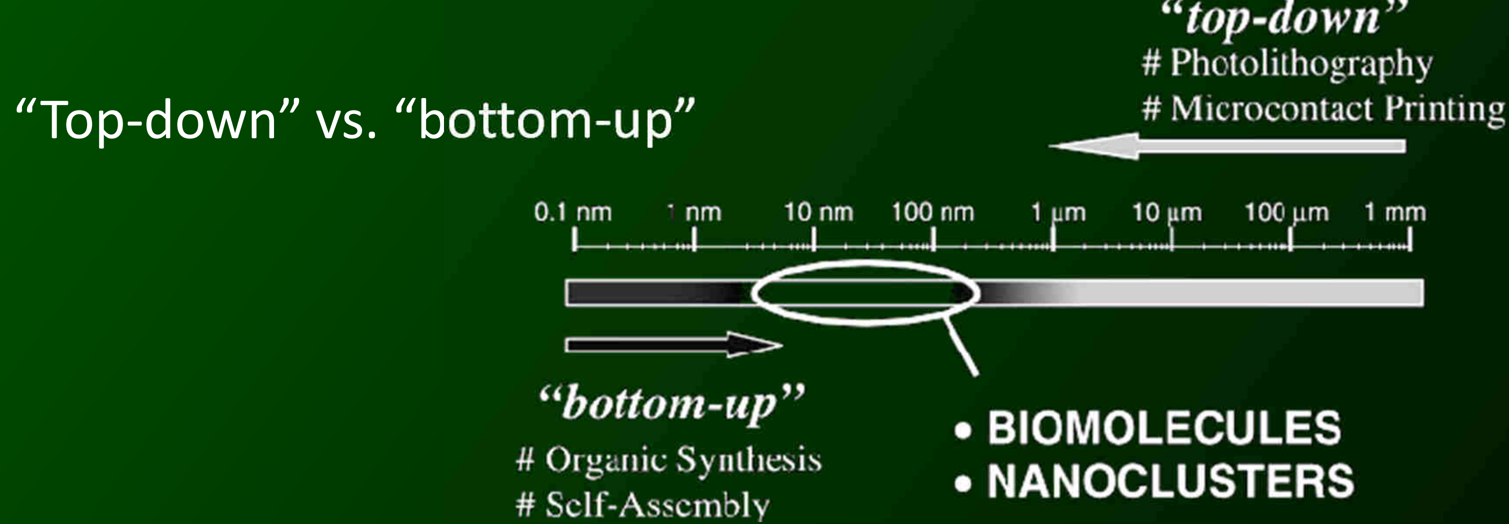


Lithography

Moore's law:

feature sizes shrank by a factor of 2 every 18 months

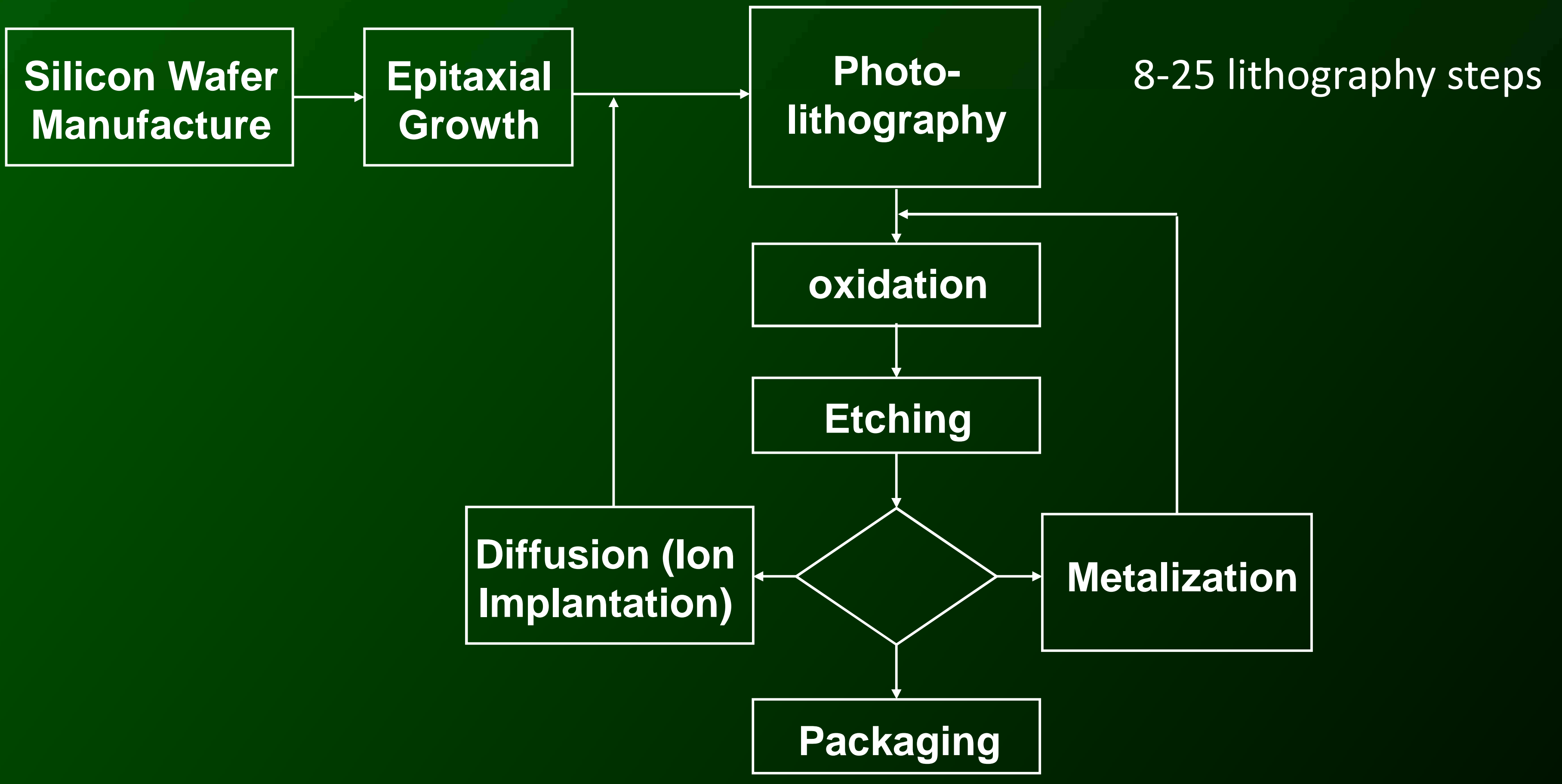
"Top-down" vs. "bottom-up"



nanolithography

UV (EUV) optical lithography
X-ray lithography
Nanoimprinting
block copolymer self-assembly
use of supercritical fluids
nonlinear two-photon lithography
electron beam lithography

Fabrication Processes for VLSI



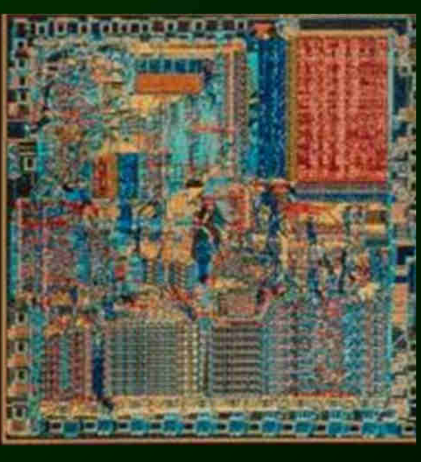
The minimum feature size (the minimum line width or line to line separation) control the number of circuits that can be placed on the chip and has a direct impact on circuit speed. The evolution of IC is therefore closely linked to the evolution of lithographic tools.

From Photo-Lithography to Chip

Computer chips are made using photolithography (using light to transfer a pattern from a photomask to a light-sensitive chemical (photoresist))

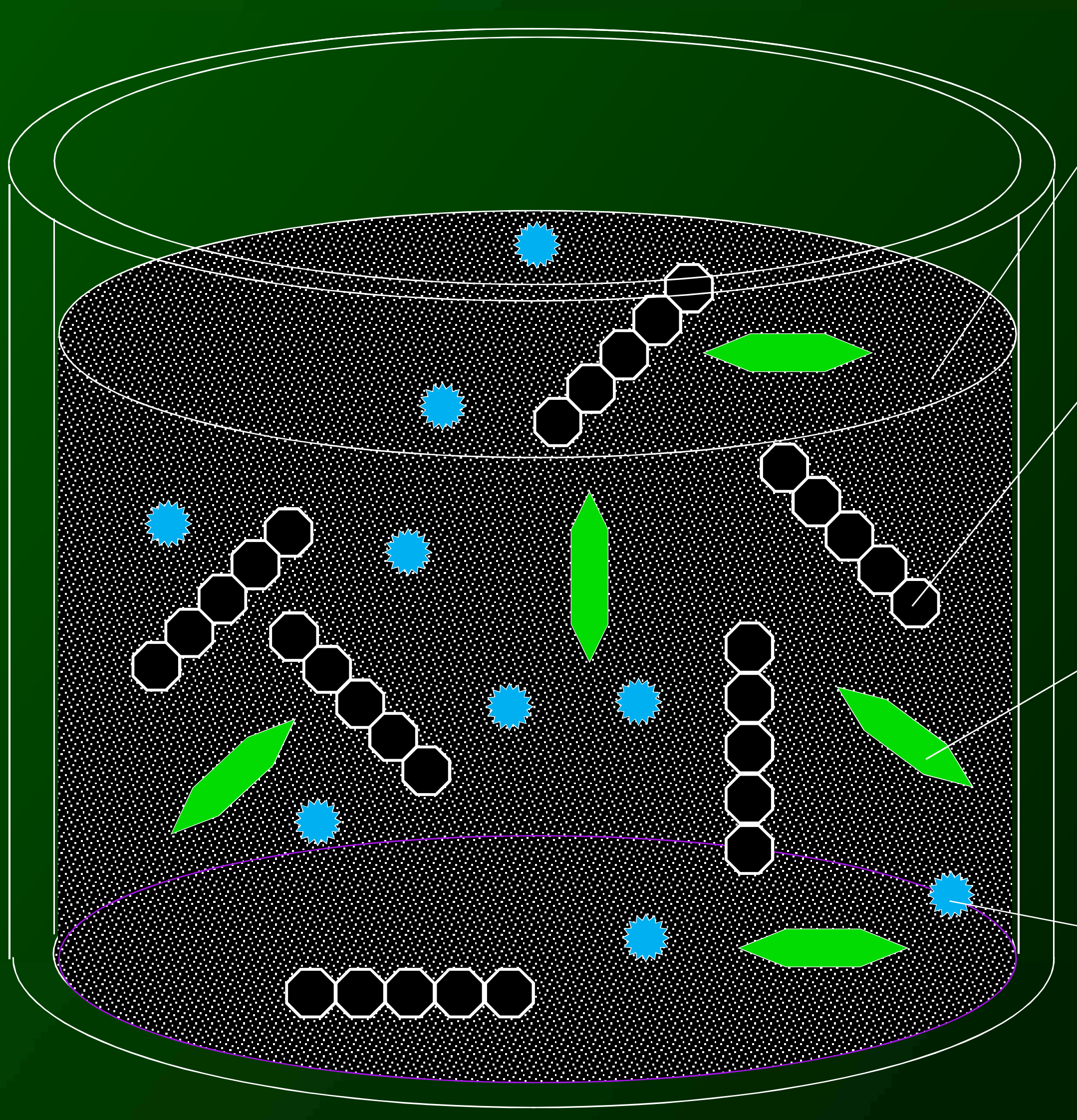
Role of the Resist:
Light exposure changes solubility and allows mask formation

Main Benefit:
High throughput!



Packaging

Conventional Photoresists



Solvent:
gives the resist its flow characteristics

Resin: mix of polymers that hold the resist together; gives the resist its mechanical and chemical properties

Sensitizers:
sensitive to light; these will react when exposed to light

Additives:
chemicals that control other aspects of the resist material

Positive vs. Negative Photoresist

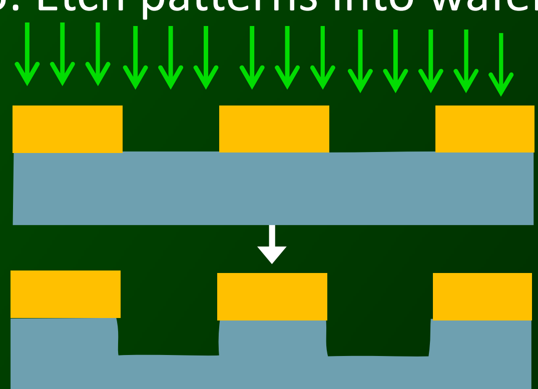
Positive Photoresist:
Exposed areas → dissolvable

Negative Photoresist:
Unexposed areas → dissolvable

3. Expose to UV light

4. Develop and rinse

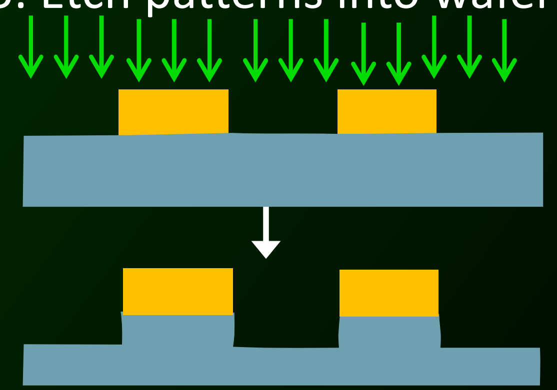
5. Etch patterns into wafer



6. Remove residual photoresist

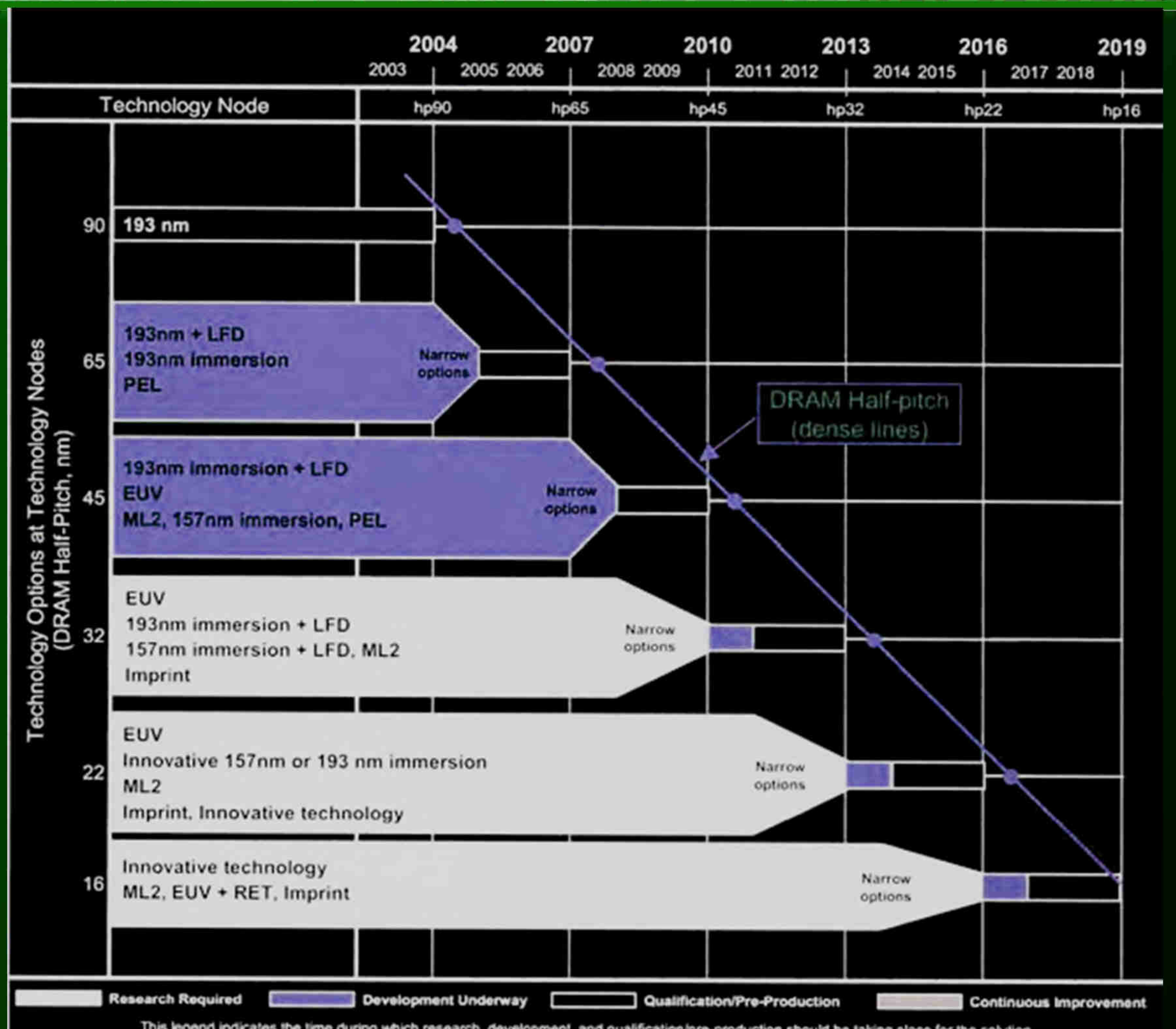
4. Develop and rinse

5. Etch patterns into wafer



6. Remove residual photoresist

Moore's Law and Lithography

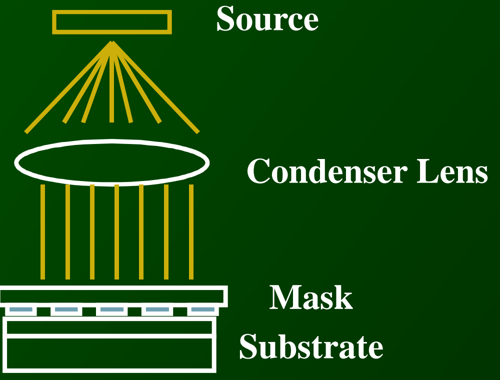


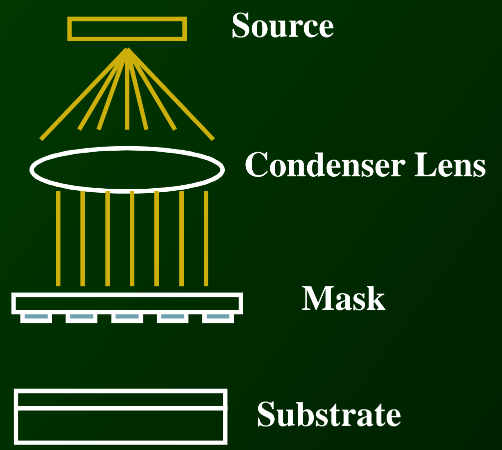
Masks

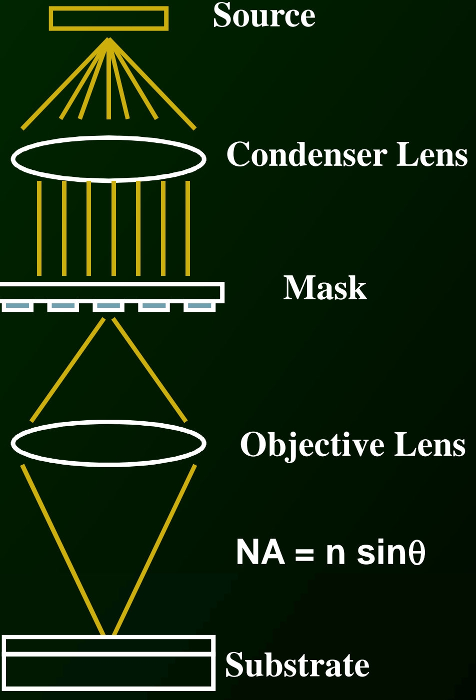
Contact Printing:
+ Simple, cheap
- Poor resolution
- Bad mask lifetime
- Defects

Proximity Printing:
+ Minimal mask damage
- Poorer resolution
- Diffraction error

Projection Printing:
+ Higher resolution
+ lens reduces diffraction error
- Optical system







UV Optical Lithography

projection lithography

2005: (65nm) $\lambda = 193$ nm

Optical lithography :

+ High throughput

+ Low cost

- Diffraction limited

$$HP = \frac{k_1 \lambda}{NA} = \frac{k_1 \lambda}{n \sin\theta}$$

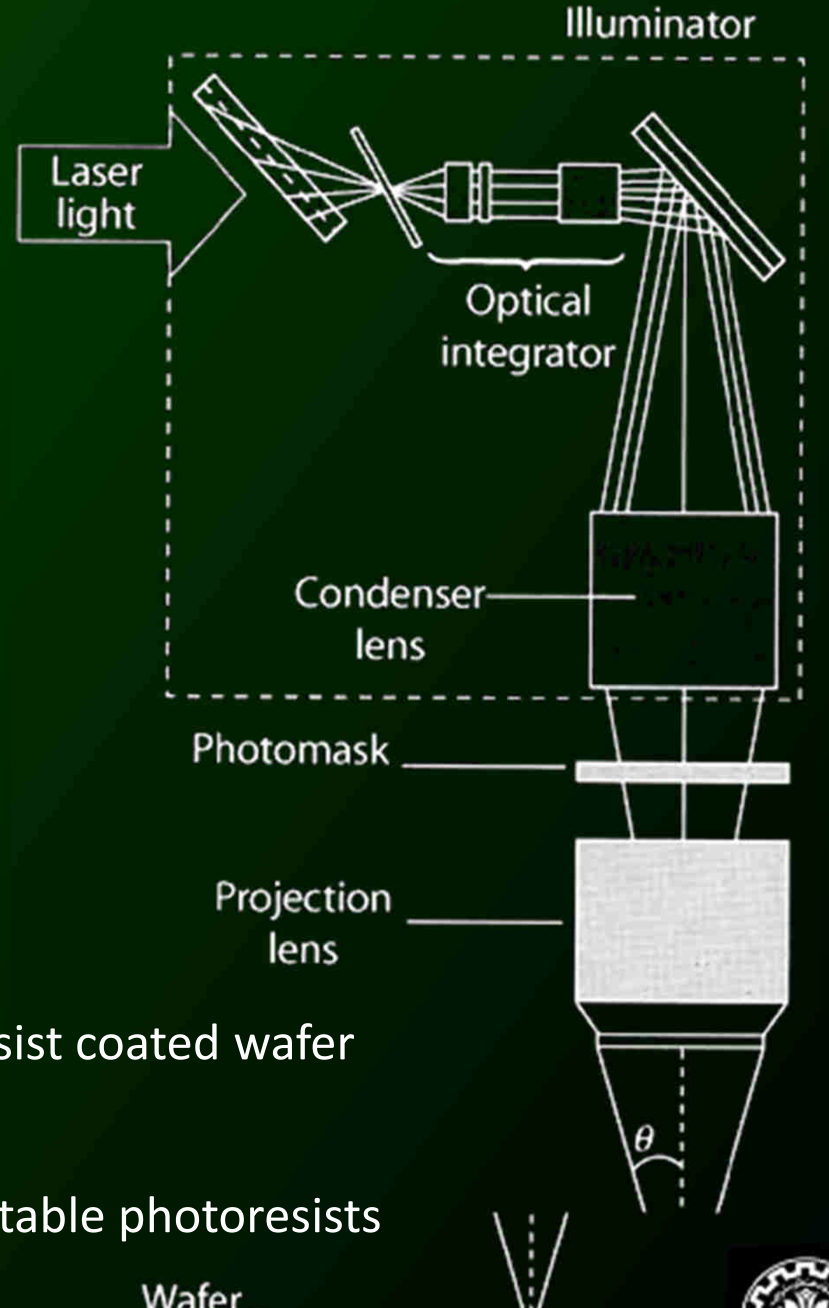
numerical aperture

θ = half-angle of the converging beam

n = refractive index of the medium above the photoresist coated wafer

k_1 = min 0.25 (~0.4)

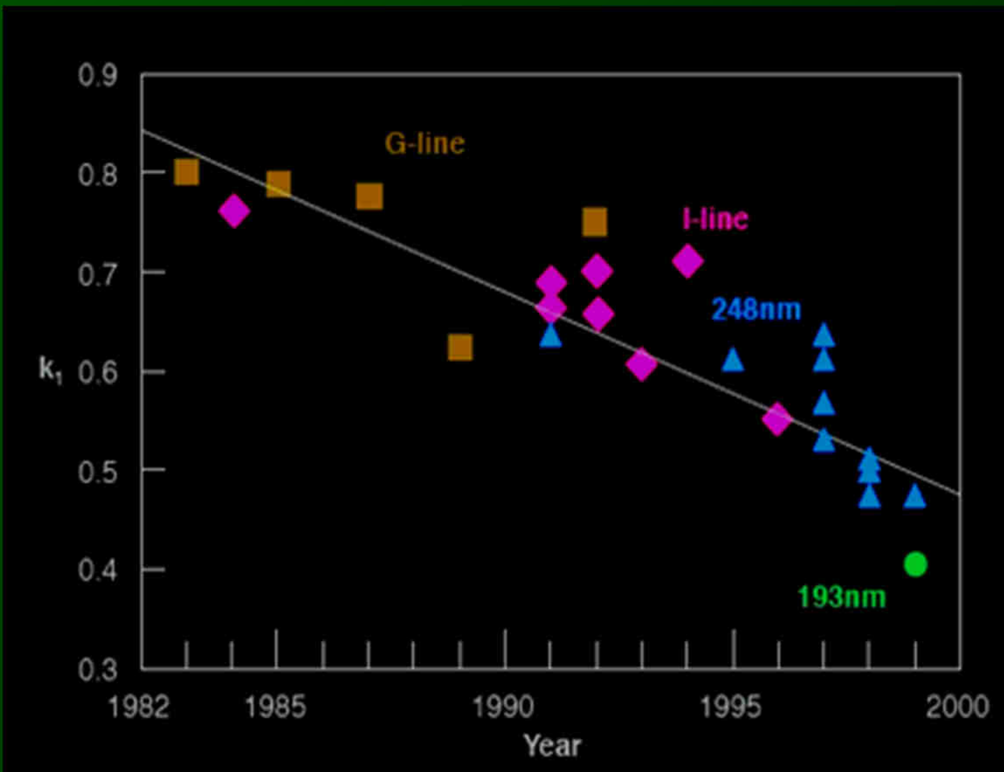
λ ↘ appropriate light sources, transparent lenses, suitable photoresists

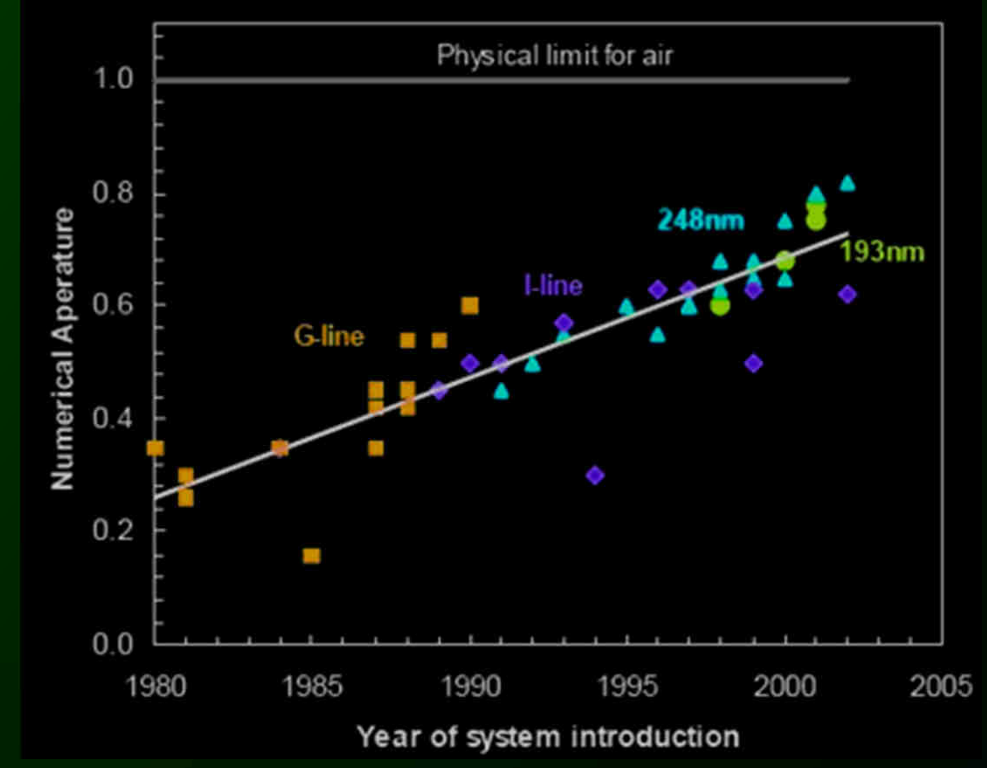


Photolithography – NA , k_1

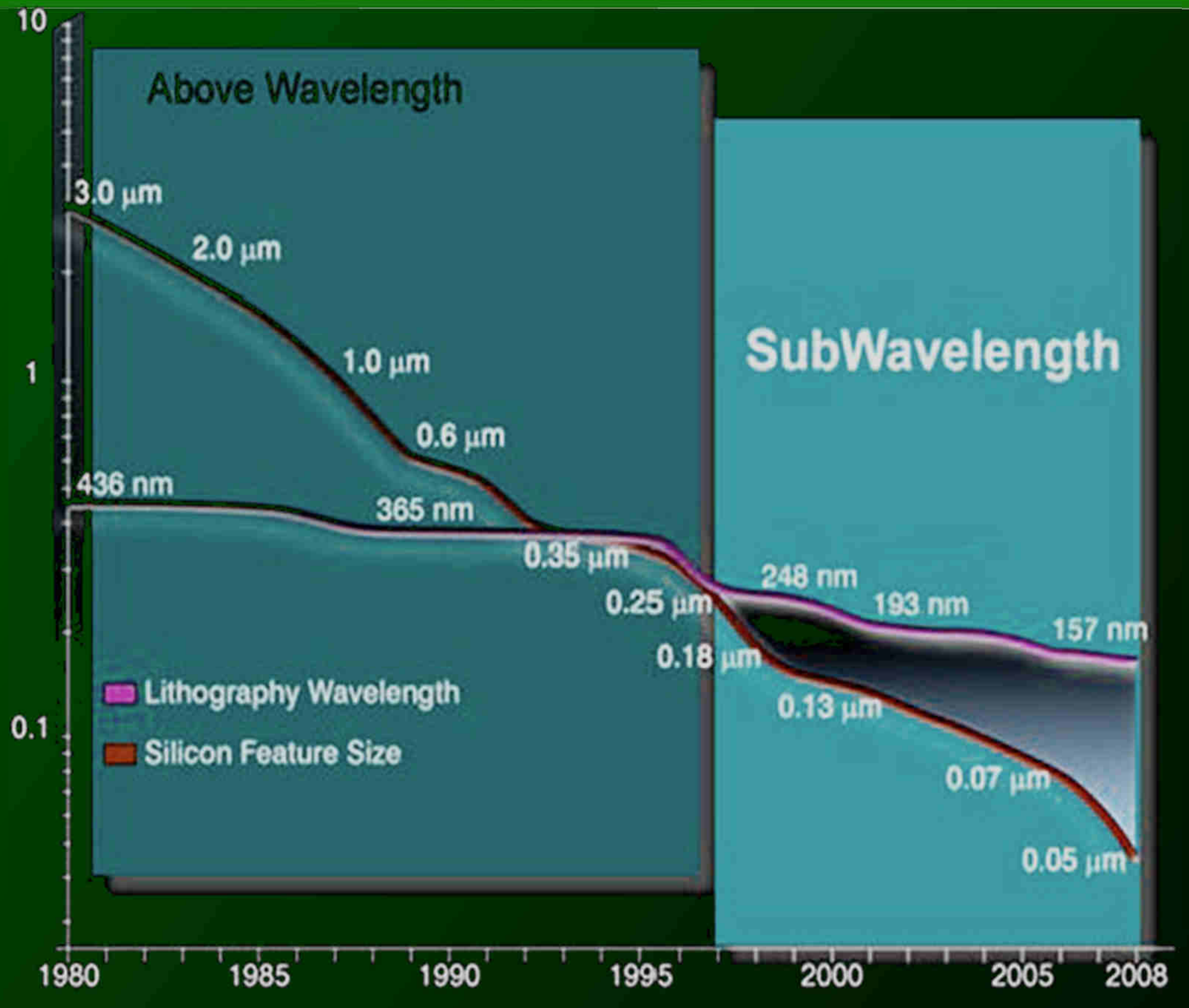
K1:
quality of the photoresist
phase shift masks
off-axis illumination
optical proximity correction

NA:
Larger lens



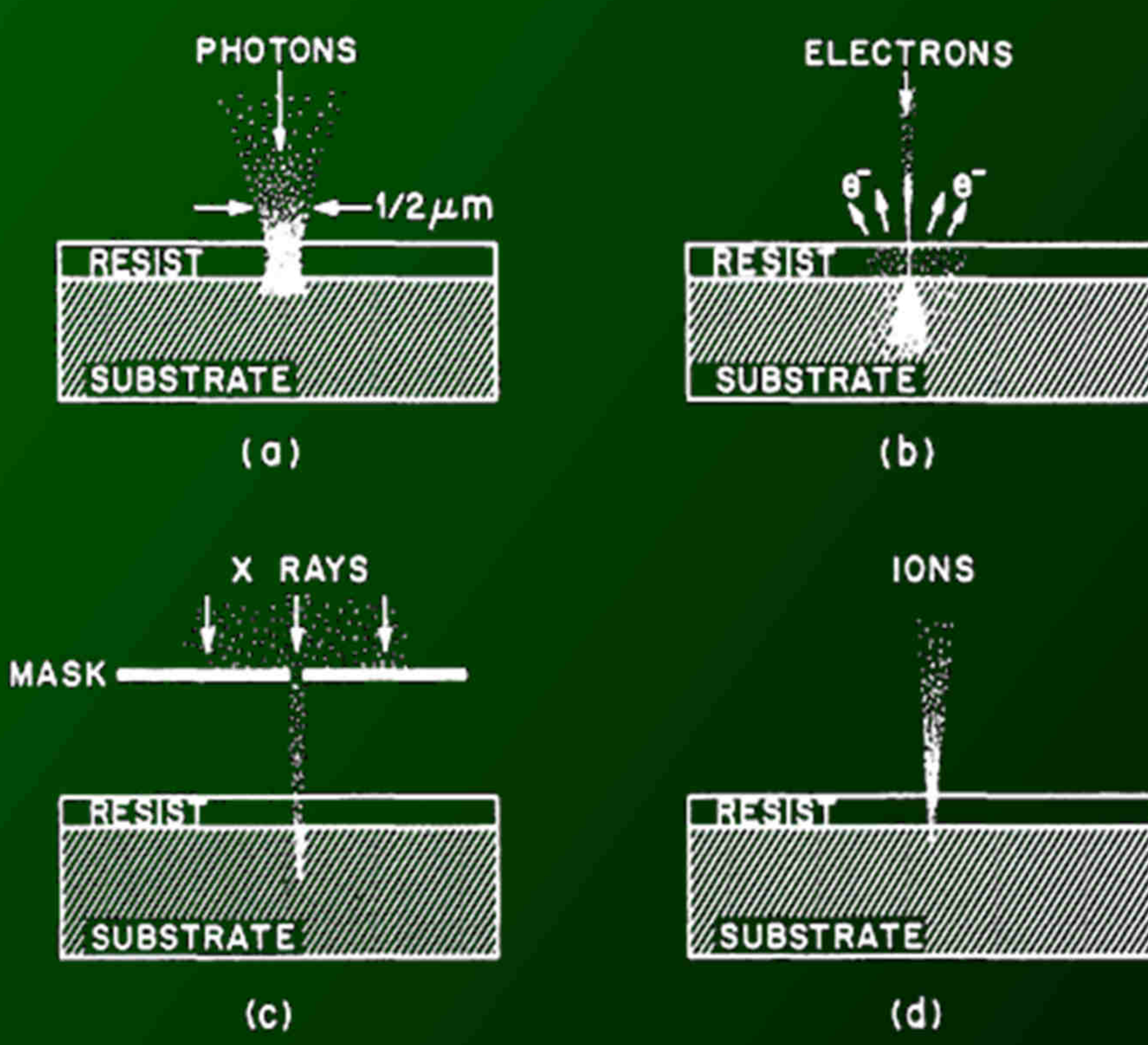


UV Optical Lithography



Subwavelength era: printing 1 inch line with 3 inch brush

Next Generation Lithography



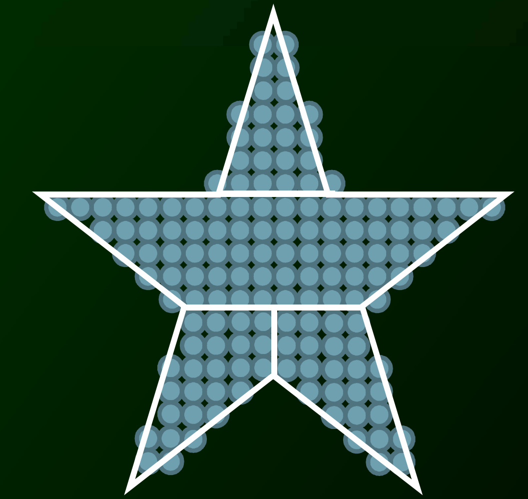
		λ	E
light	UV	400 nm	3.1 eV
	Deep UV	250 nm	4.96 eV
	X-ray	0.5 nm	2480 eV
Particles	Electrons	0.62 A°	20 KeV
	Ions	0.12 A°	100 Kev

EUV Lithography

Laser plasma source or synchrotron radiation
EUV light 10–14 nm
Paraboloid
Reflection mask
Ellipsoid
Ellipsoid
Plane
Wafer
1 m

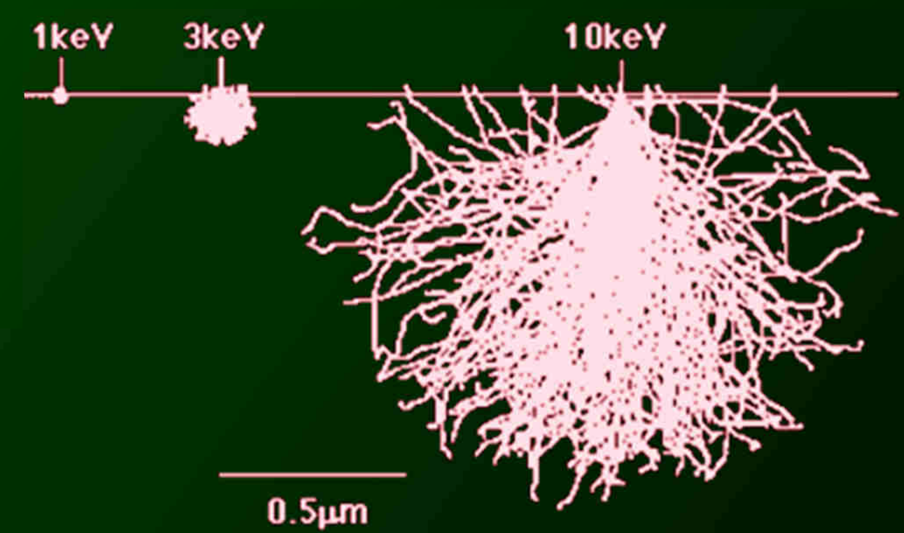
- Uses very short 13.4 nm light
- All reflective optics (at this wavelength all materials absorb!)
- Uses reduction optics (4 X)
- Step and scan printing
- Optical tricks seen before all apply: off axis illumination (OAI), phase shift masks and OPC
- Vacuum operation
- Laser plasma source
- Very expensive system

Electron Beam Lithography

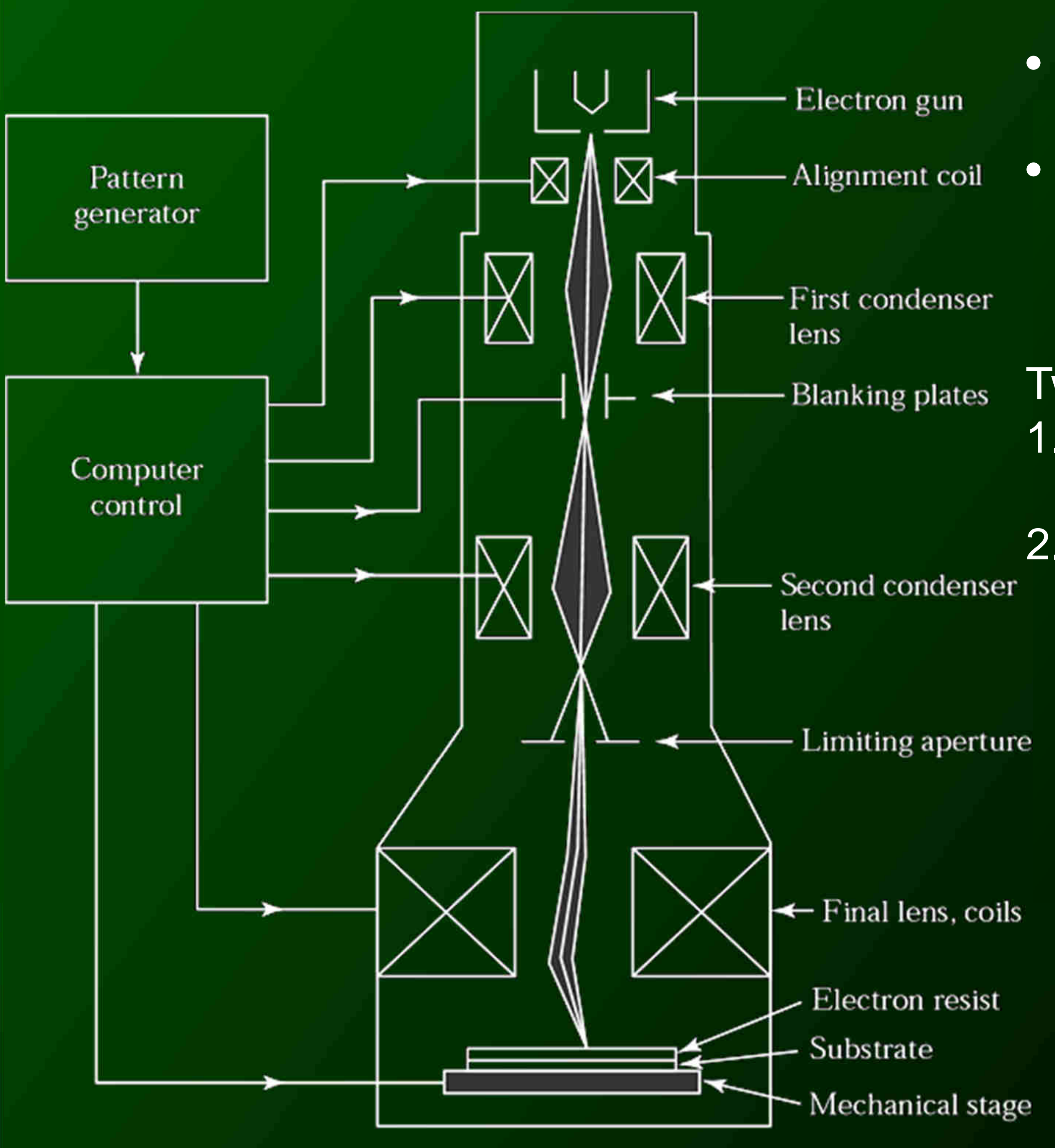


+ Highest resolution of mainstream litho. tech.
+ Flexibility (no mask required)
+ Simplified resist processing

- Exposure needs to be done in vacuum.
- Substrate charging/damage
- Throughput!



Schematic of an EBL machine



- Diffraction is not a limitation on resolution
- Resolution depends on electron scattering and beam optics the size of the beam, can reach ~ 5 nm

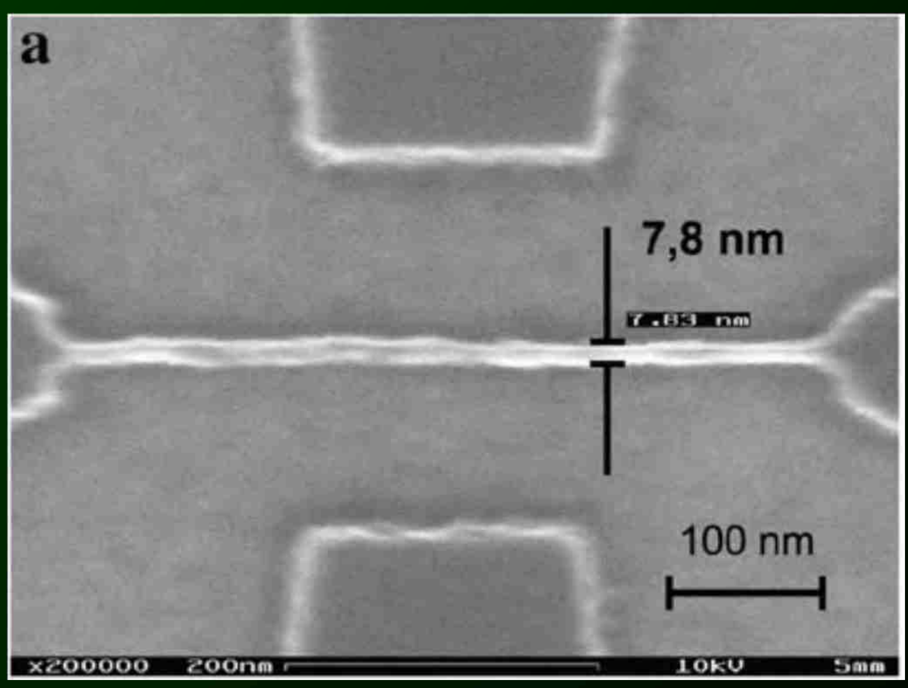
Two modes of operation:

1. Direct writing with narrow beam
2. Electron projection lithography using a mask :EPL

Electron Beam Lithography

about 10 nm

low-energy electrons
a high-resolution resist (calixarene)
slow serial writing



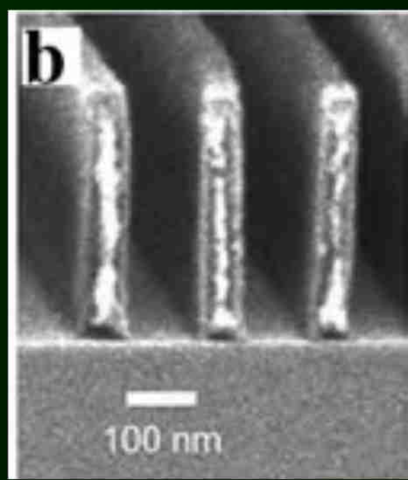
hexaacetate p-methylcalixarene (MC6A0Ac)
resists using a 10 keV electron beam

Proton-Beam Writing

MeV protons

more massive protons:
straight path, 3D, high aspect ratio structures with vertical, smooth sidewalls (Fig. 3.64b), and lateral resolutions down to 22 nm

$$m_p = 1800 m_e$$

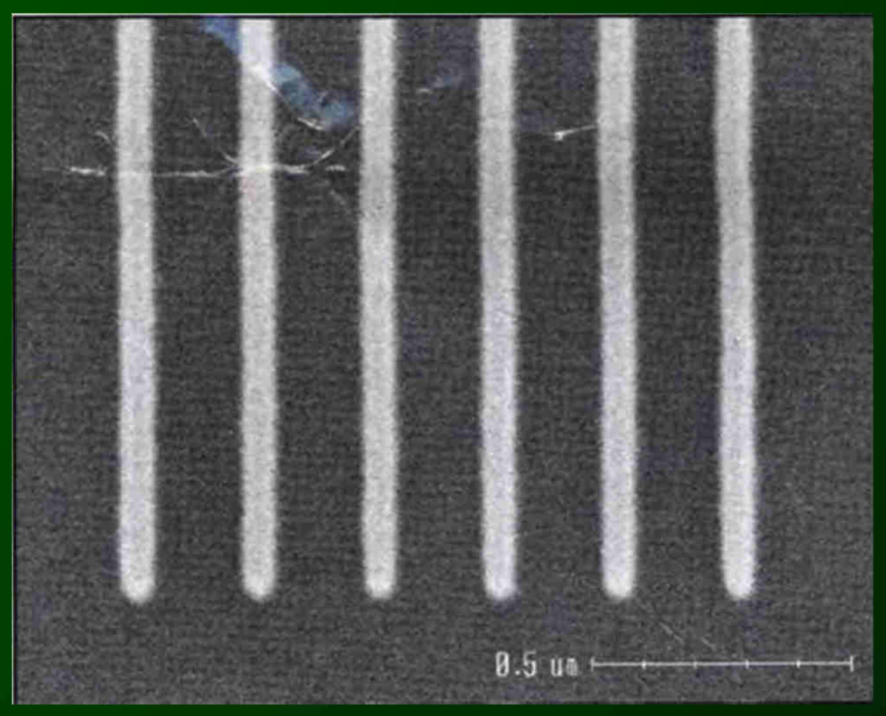


2 MeV proton beam

Nano-imprint Lithography (NIL)

low-cost, high-resolution patterning technique (sub 45nm)

patterns can be repeatedly transferred from a mold to some polymeric material with a 5-nm horizontal patterning resolution



UV-NIL

(1) Dispense

imprint mold

(2) Fill & Expose

UV light

(3) Separate

residual layer

(4) Etch Process

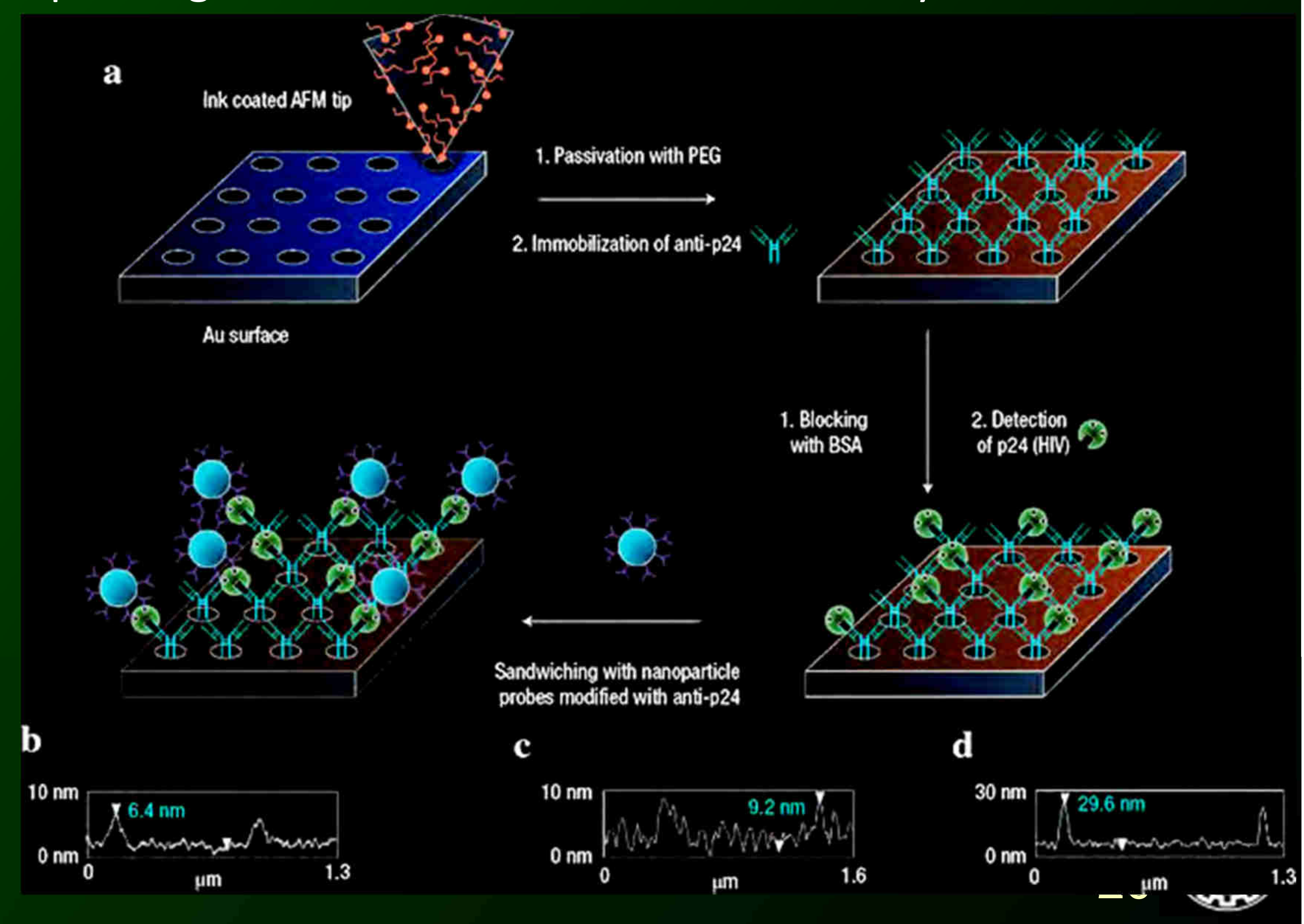
processing flow of ultraviolet-assisted nanoimprint lithography (UVNIL)

Dip-Pen Nanolithography (DPN)

scanning probe microscopy-based nanofabrication technique
uses an “ink”-coated AFM tip to pattern a surface with a sub 50nm resolution and without pre-modification of the surface.

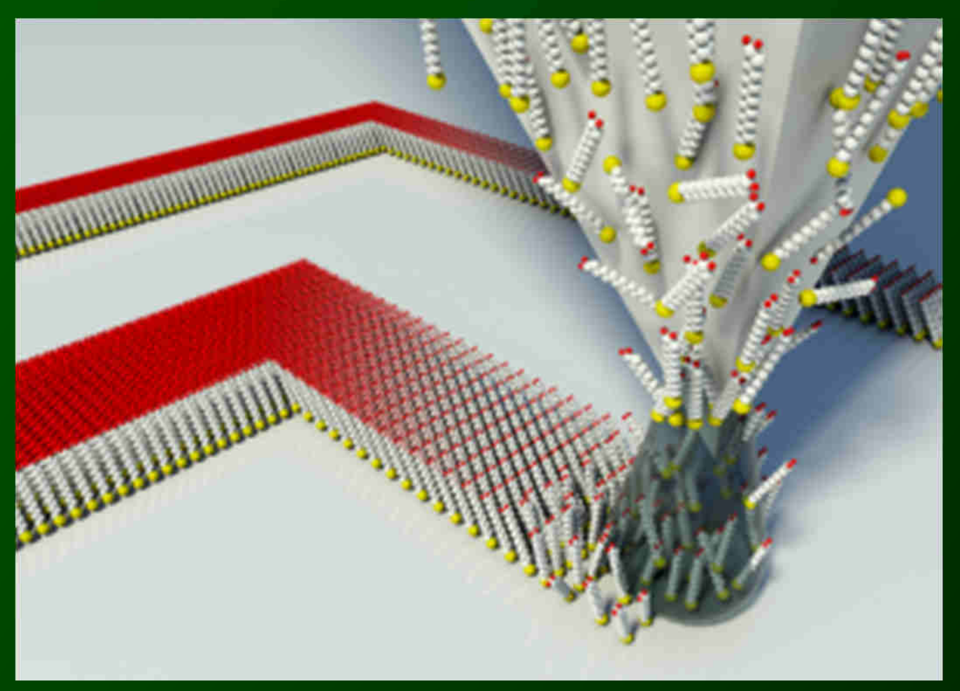
a versatile tool for depositing soft and hard materials on a variety of surfaces

Inks: small organic molecules, polymer, DNA,proteins, nanoparticles, and metal ions

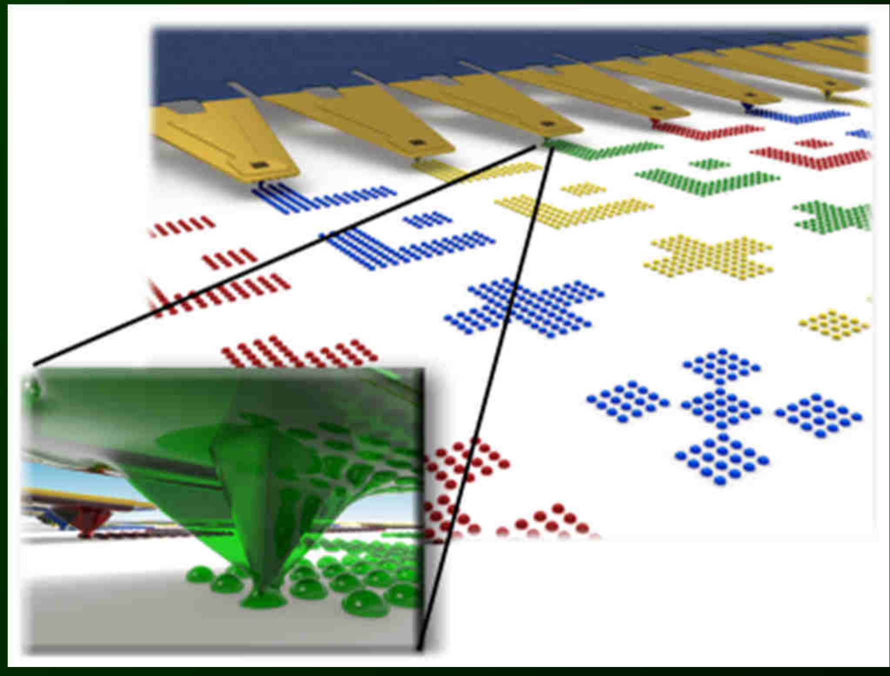


Dip-Pen Nanolithography (DPN)

Molecular inks



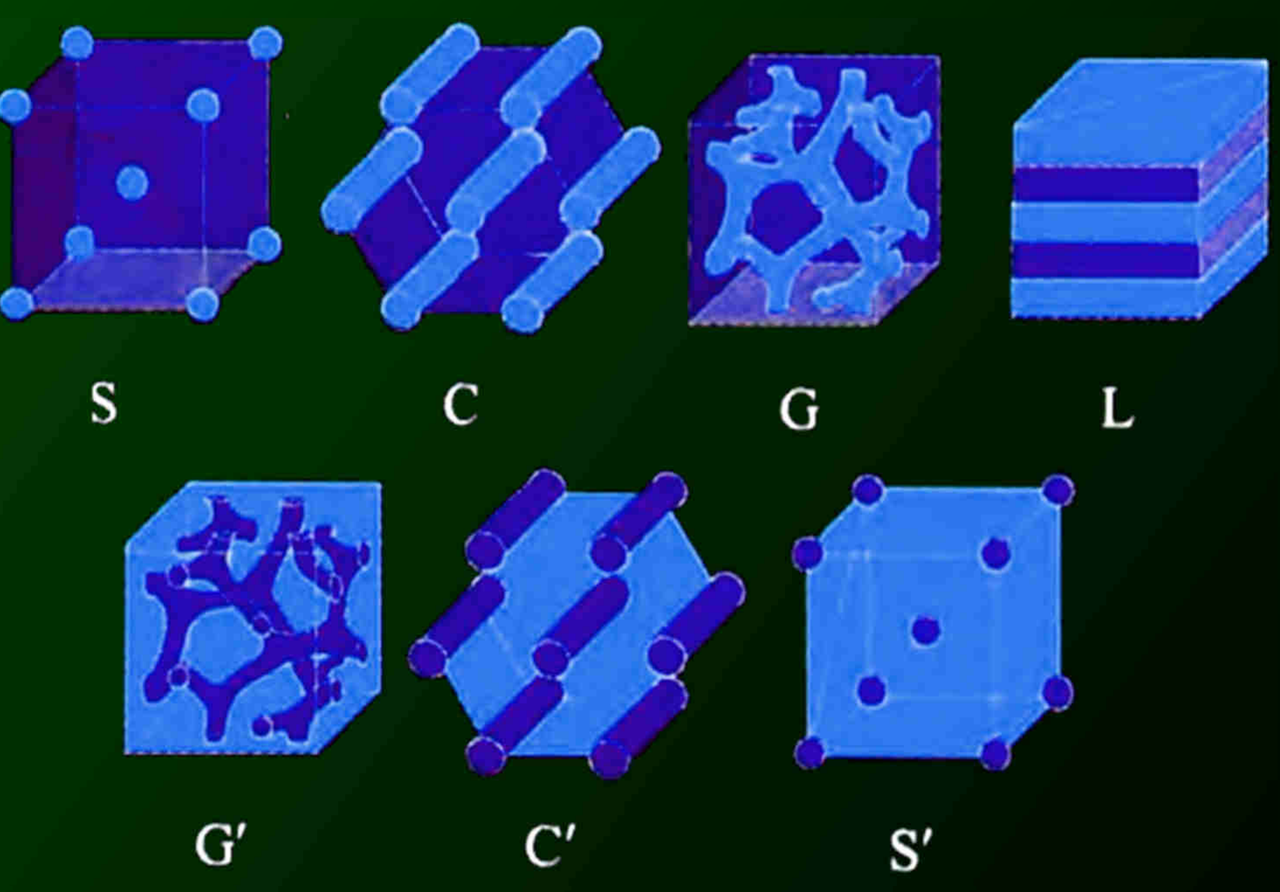
Liquid inks



Block Copolymer Lithography

"bottom-up" combined with conventional "top-down" (less than 45 nm)

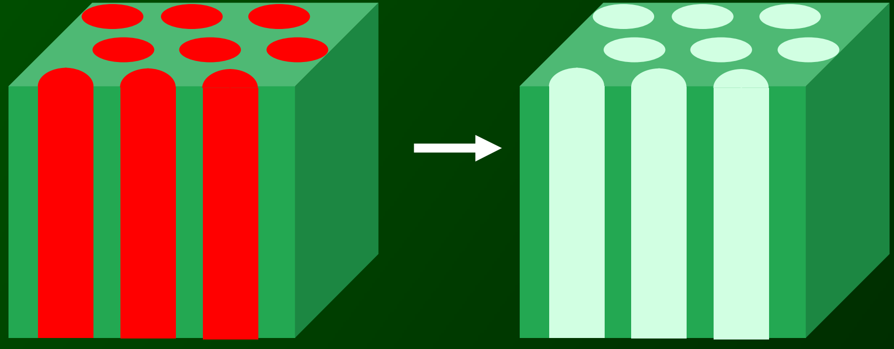
In block copolymers two chemically dissimilar polymer chains are covalently linked together at one end.

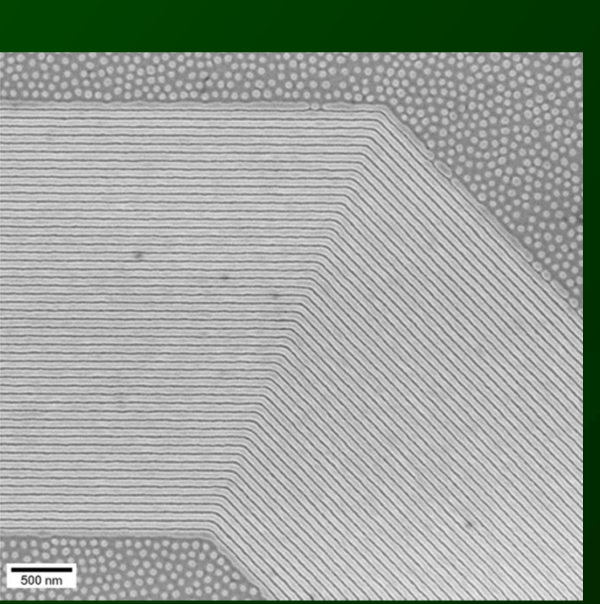


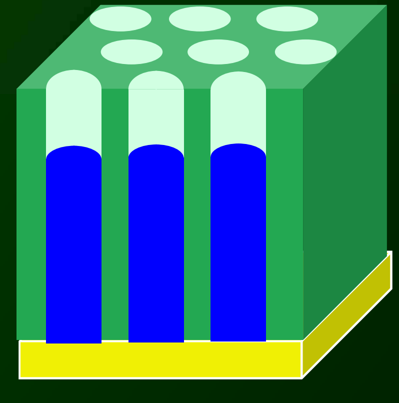
nanodomain morphologies of diblock copolymers: spherical (S, S) , cylindrical (C, C) , gyroid (G,G) , lamellar (L)

Block Copolymer Lithography

Remove polymer
block within cylinders
(expose and develop)

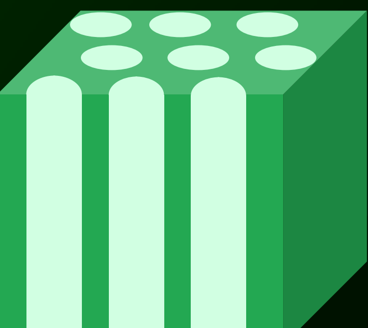






(physical or electrochemical)

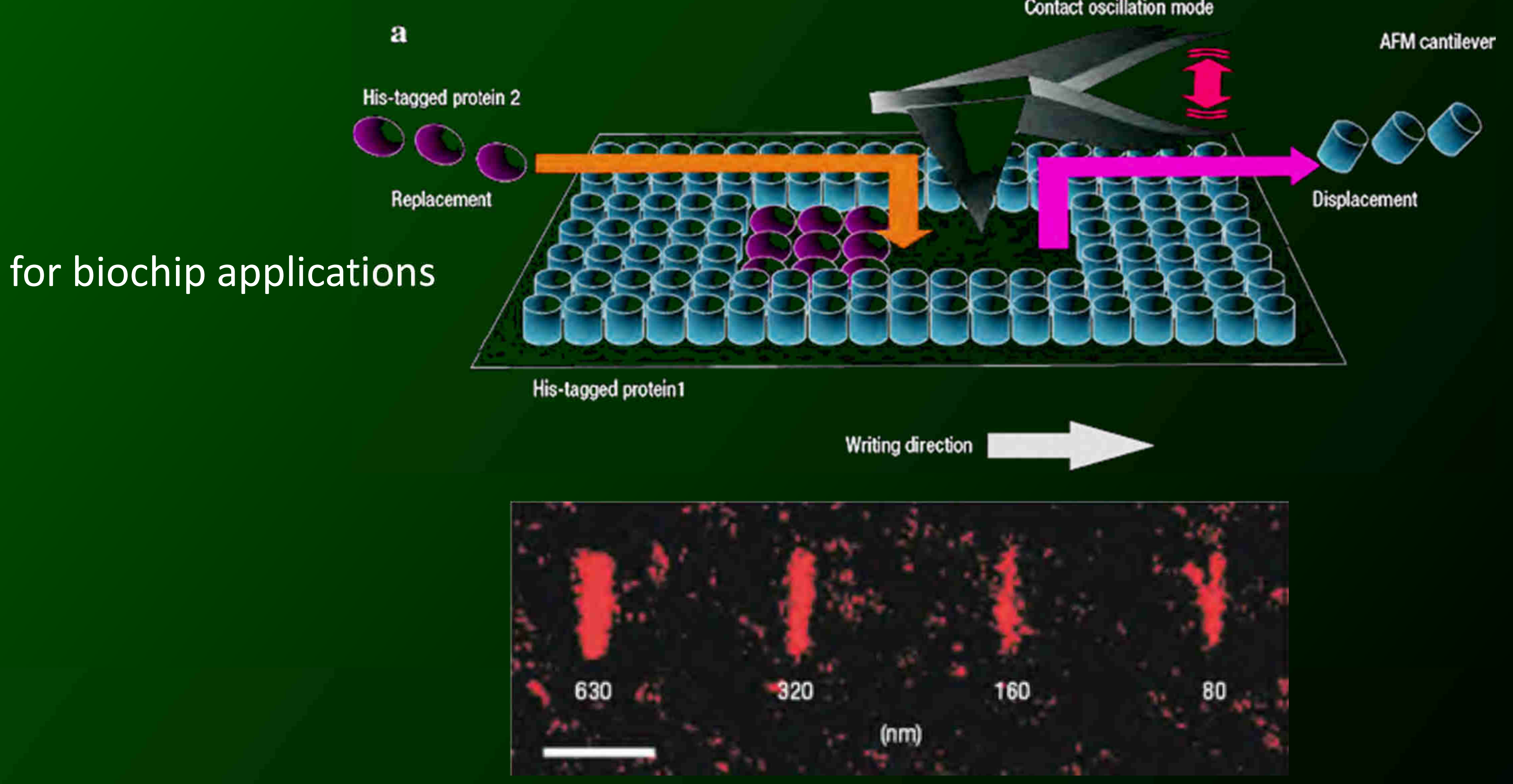
Etching
Mask



Nanoporous
Membrane

Protein Nanolithography

advantages for sensing biomedical protein–protein interactions, due to short diffusion times, parallel detection of multiple targets, and the requirement of only tiny amounts of samples

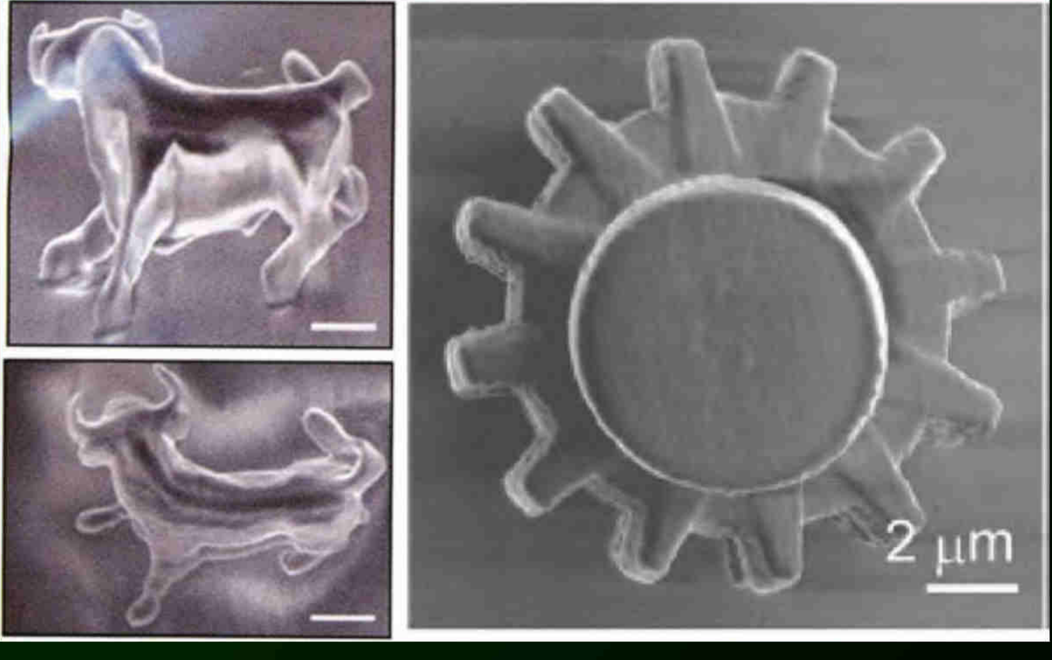


for biochip applications

Two-Photon Lithography for Microfabrication

two-photon absorption processes in certain chromophores that can simultaneously absorb two photons to produce a photochemical reaction characteristic for radiation of twice the energy.

Outside the focal point, the incident light is below the absorbance threshold. Therefore, by tightly focusing a femtosecond laser beam into a resin, photo-induced reactions such as polymerization occur only close to the focal point allowing the direct writing of 3D patterns by sample scanning.



commercial two-photon resin: SCR 500

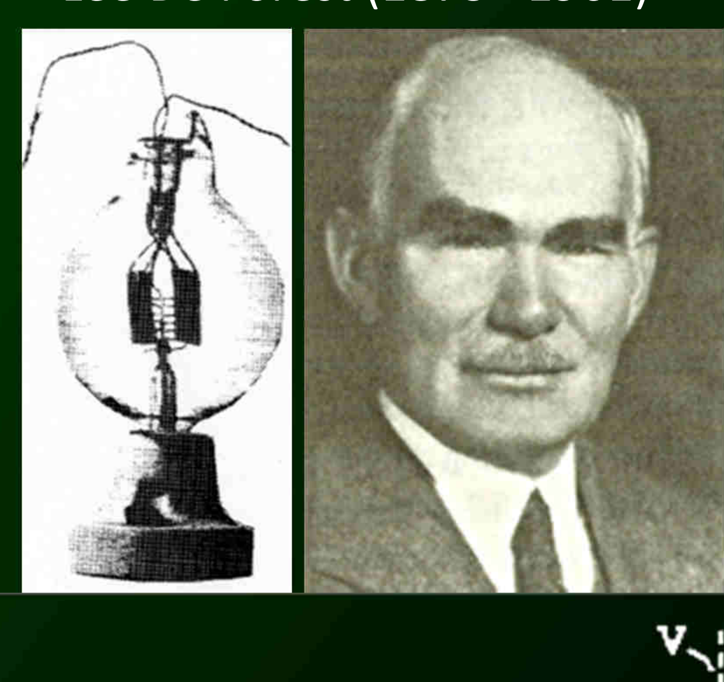
Session 2: VLSI

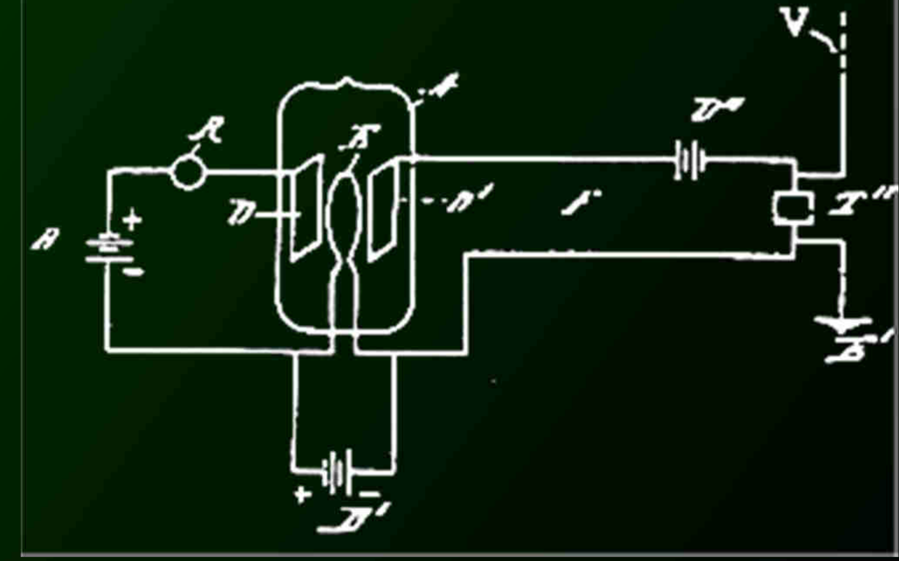
Nano Technology

(1906) Vacuum Tube : Triode

The 1946 ENIAC computer used 17,468 vacuum tubes and consumed 150kW of power

Lee De Forest (1873 –1961)





Field Effect Transistor

Julius Edgar Lilienfeld (1882 –1963)

DEVICES FOR CONTROLLED ELECTRIC CURRENT,
Filed March 28, 1928

Oskar Heil (1908 – 1994)

British patent of 1935

Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig.1.

Cu_2S

S

D

Al_2O_3

Al

G

CTS

12 Copper Sulfide

11 Aluminum Oxide

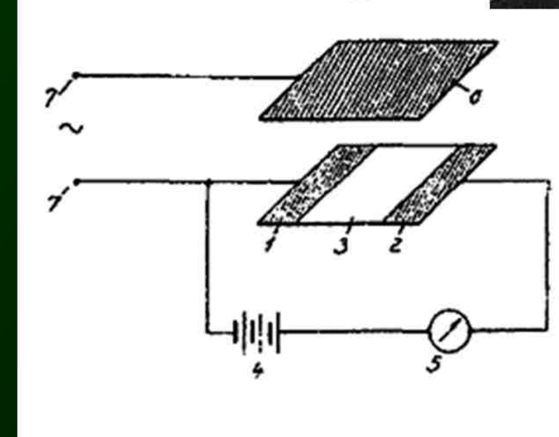
10 Aluminum

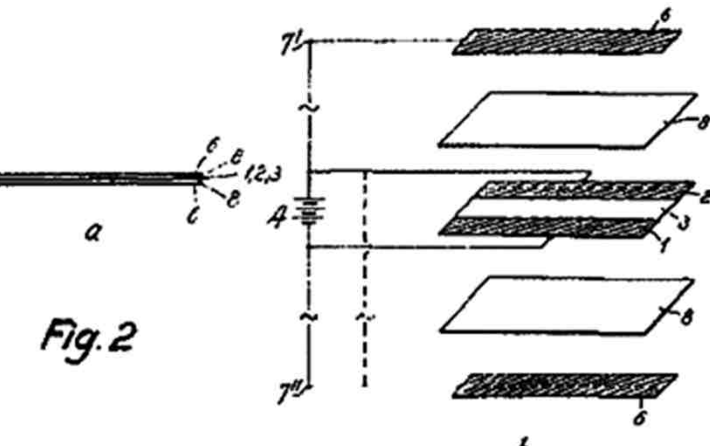
Fig.2.

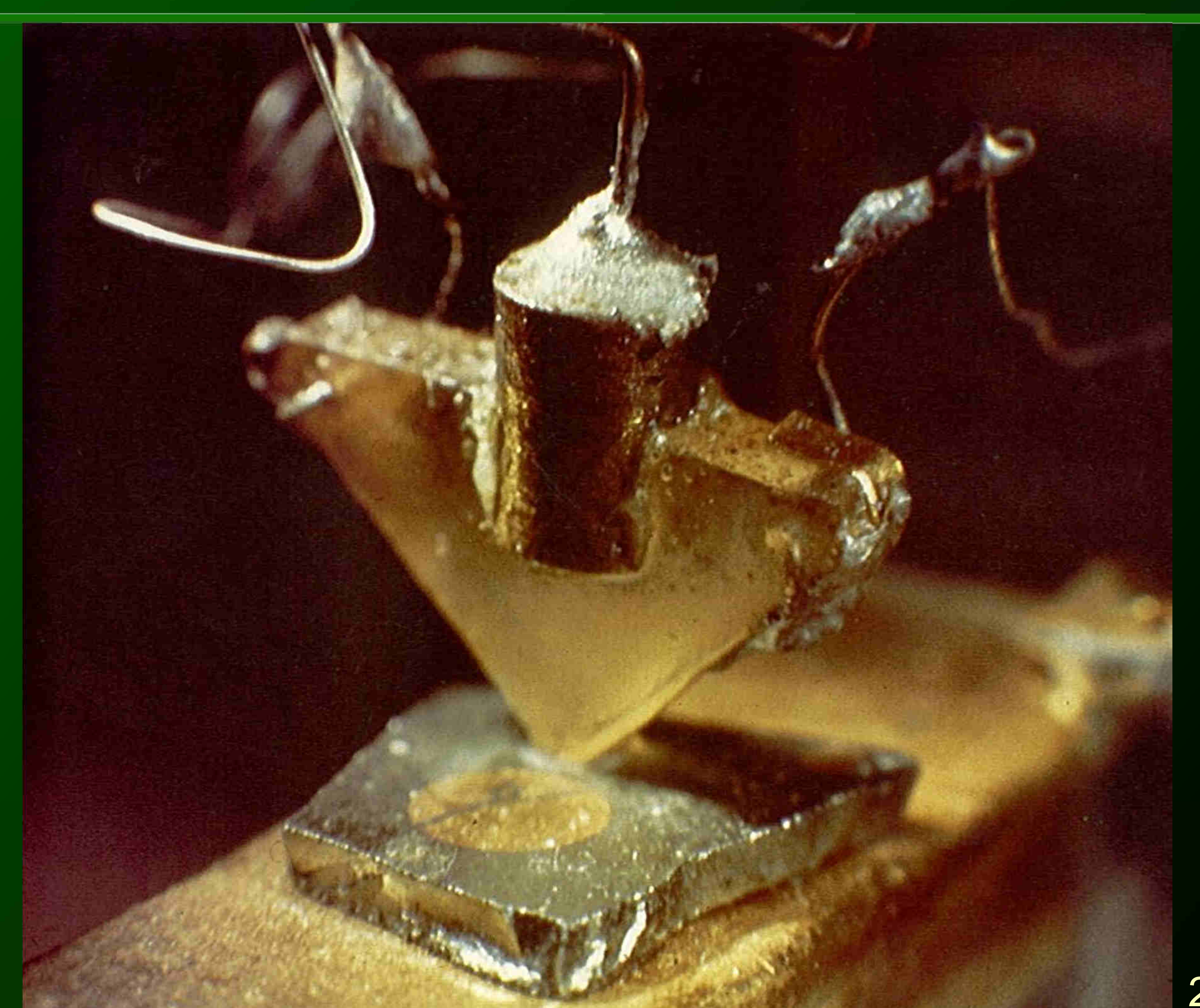
S

D

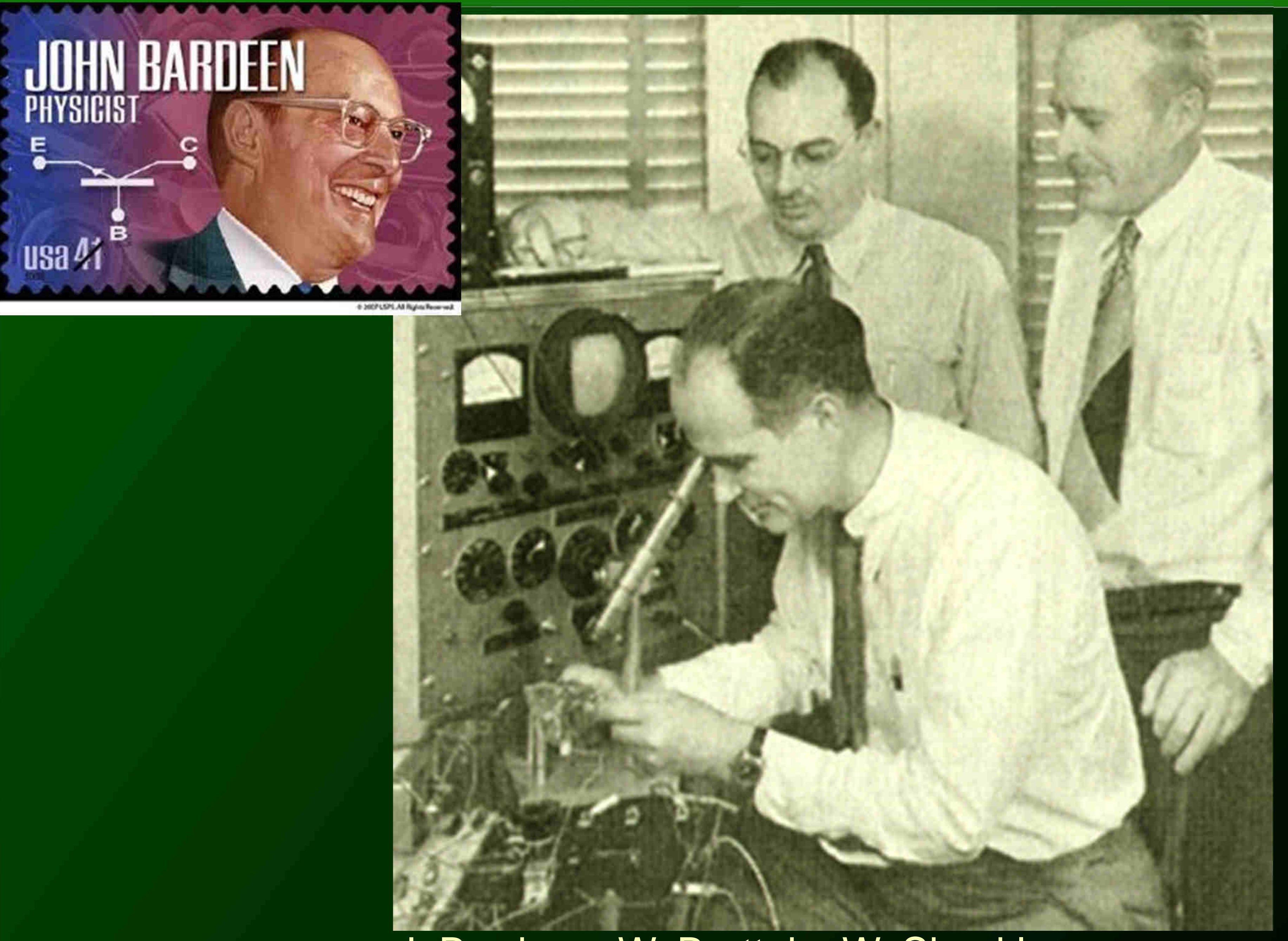
G







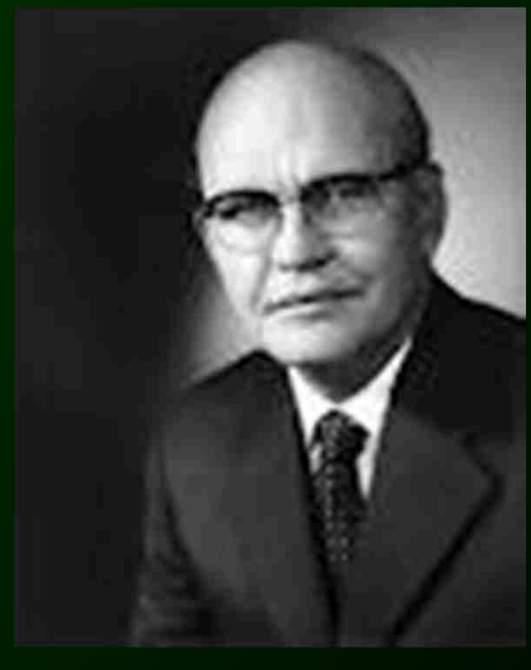
Bell Labs, 1948



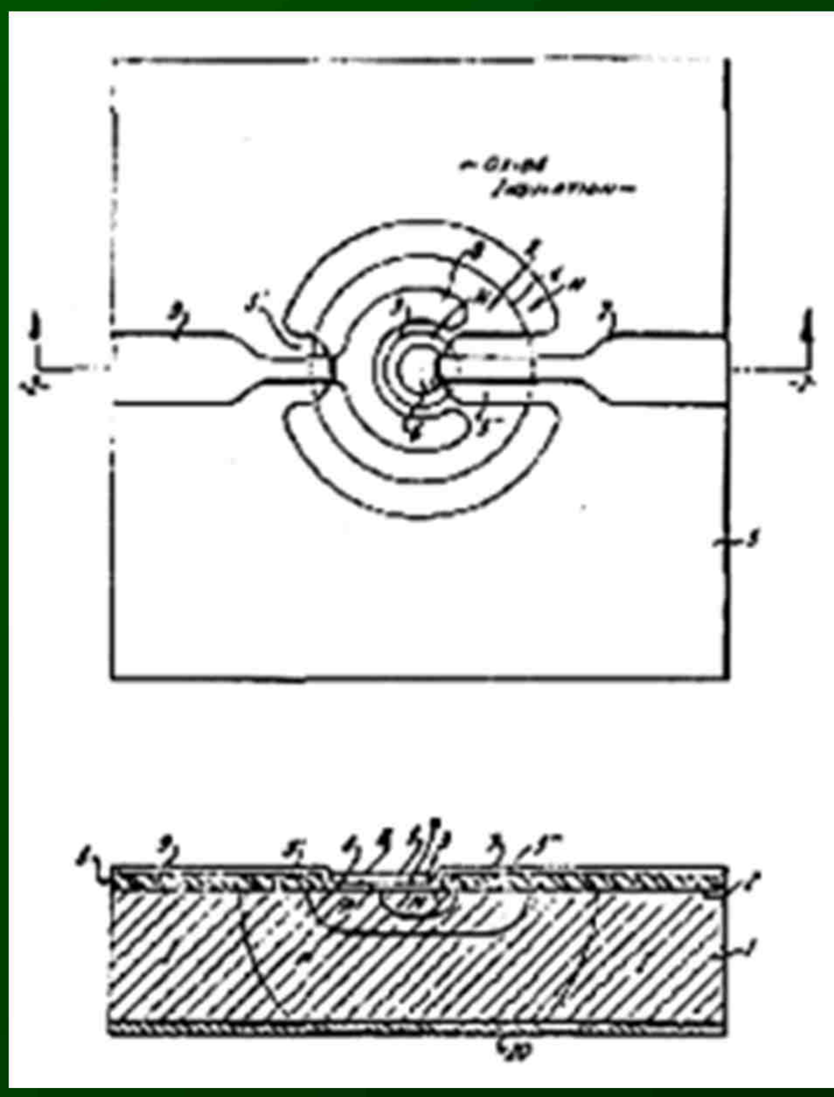
J. Bardeen, W. Brattain, W. Shockley

1958, Kilby, Texas Instruments

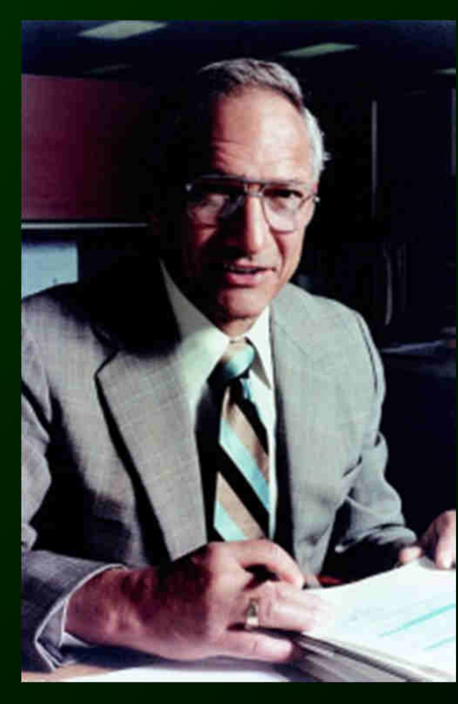
Jack St. Clair Kilby
(1923 – 2005)



1960, Noyce, planar integrated circuit

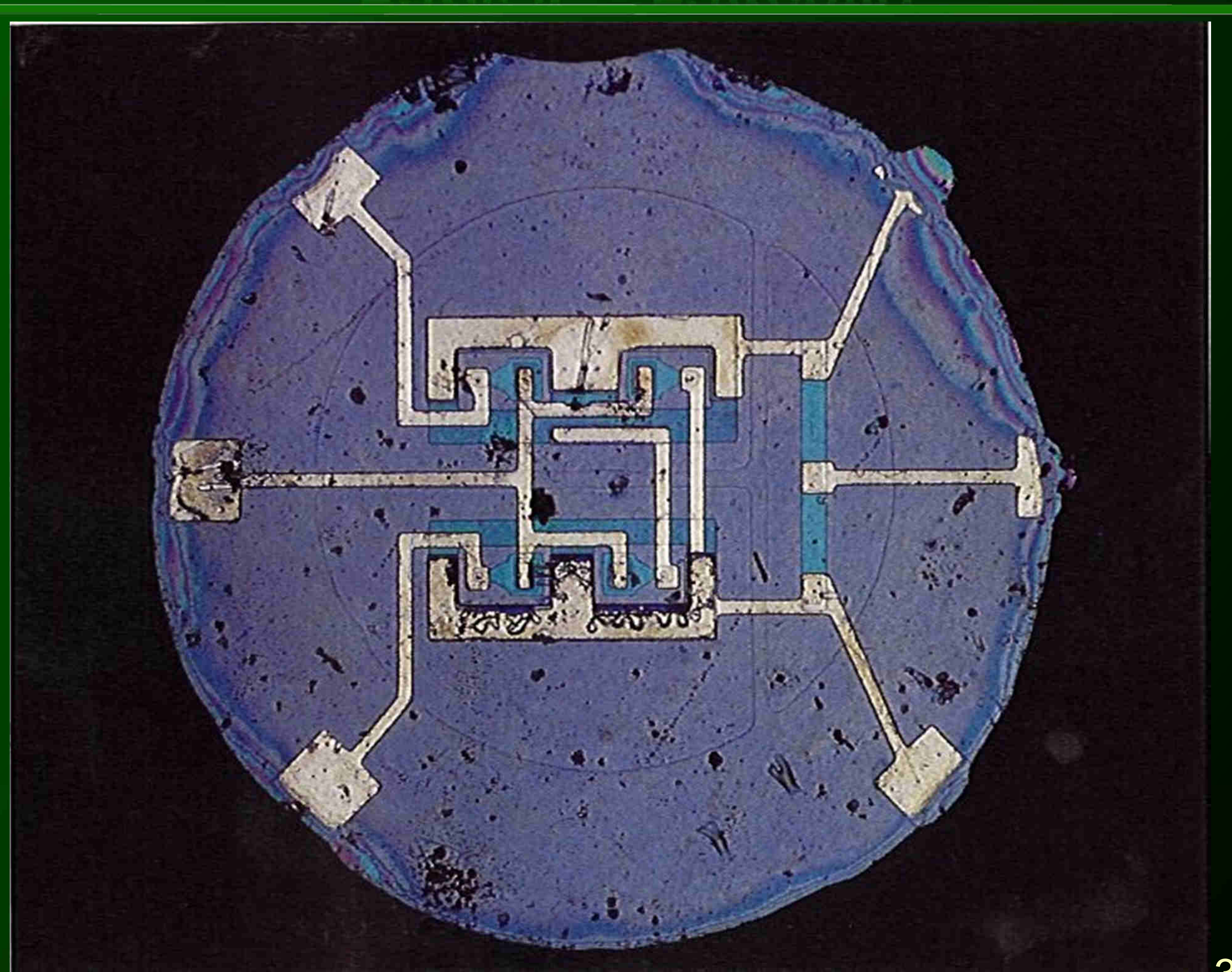


Robert Norton Noyce(1927 –1990)



Co-founder of Fairchild Semiconductor and Intel

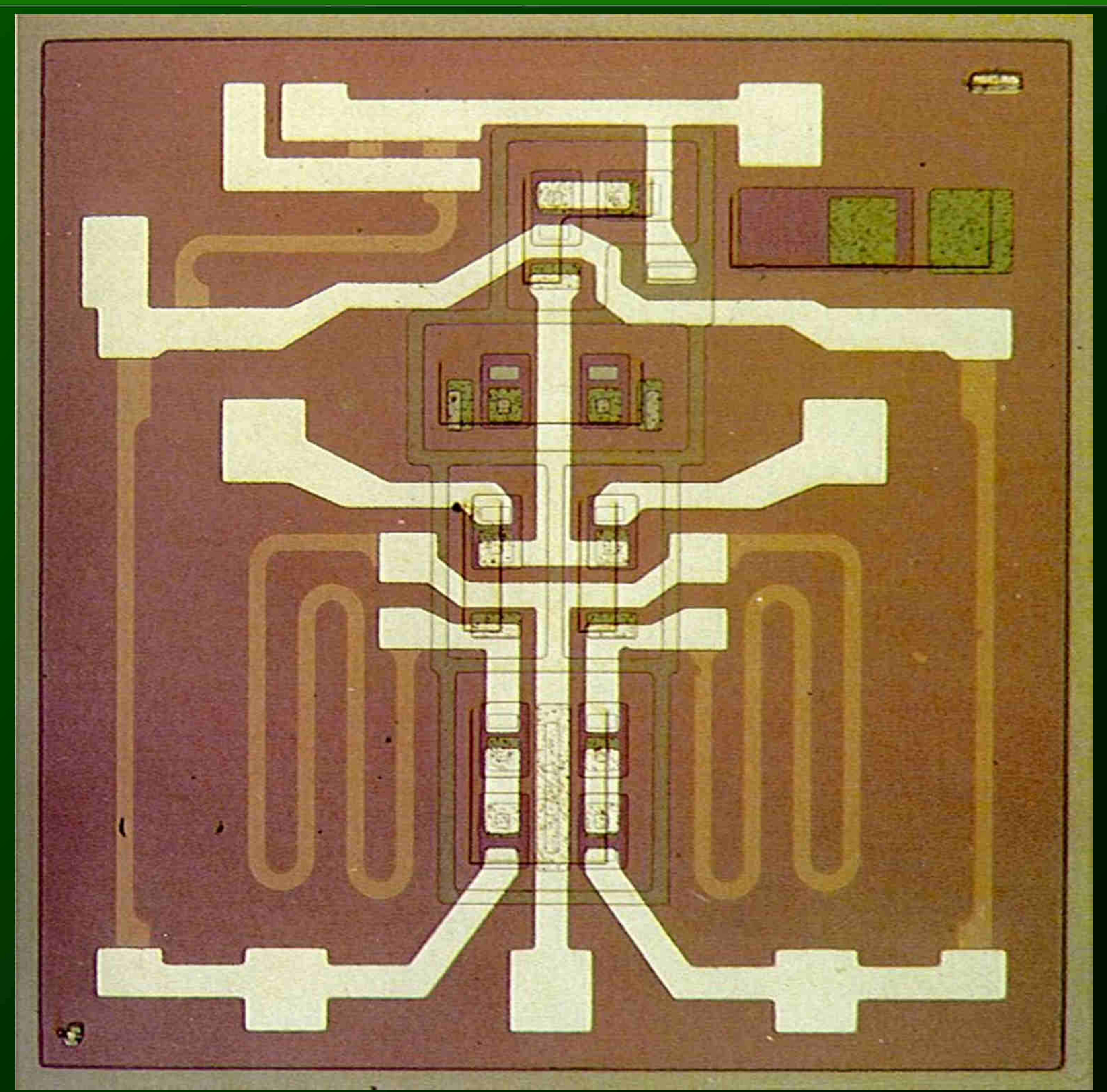
Early IC - Fairchild



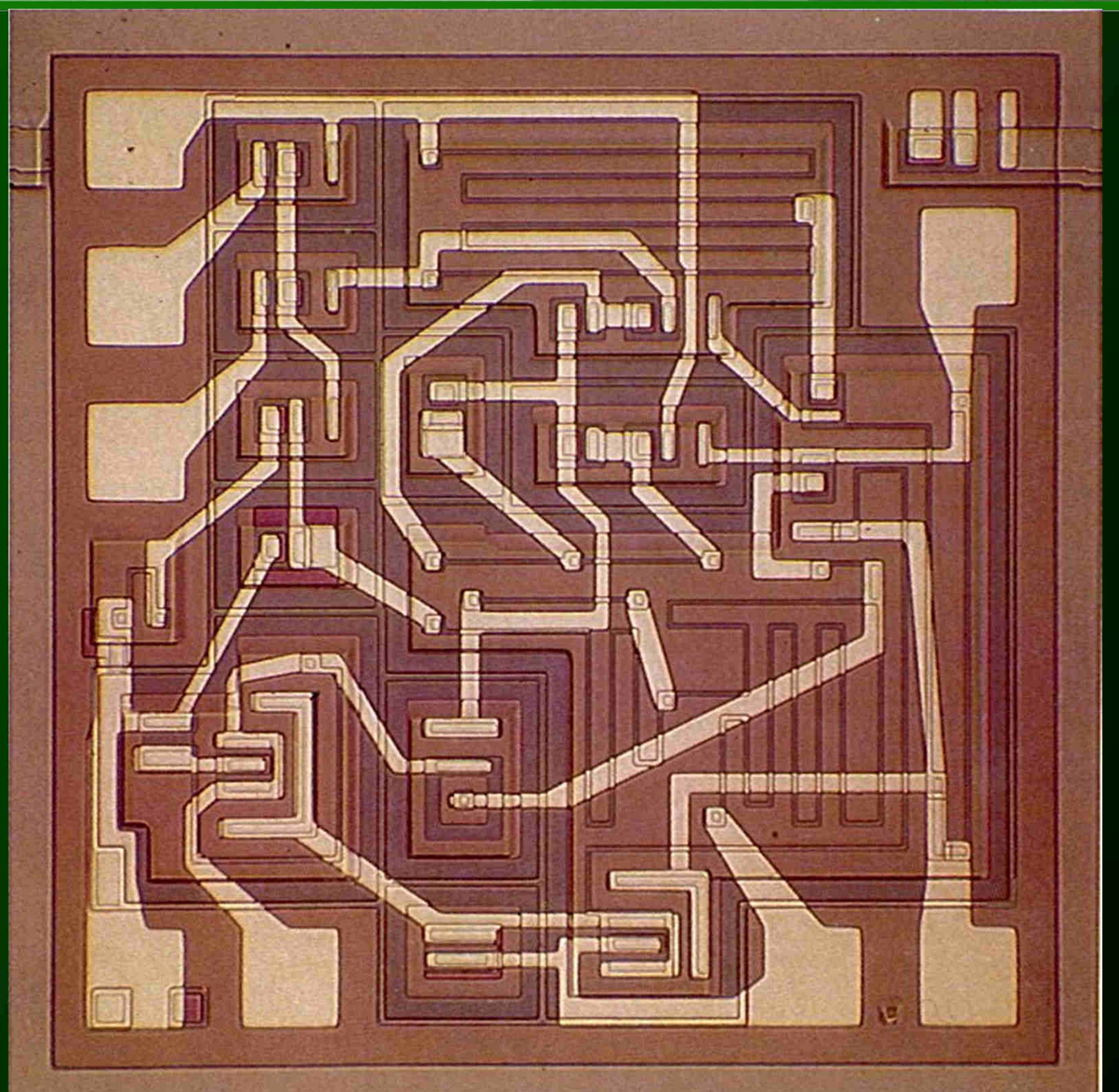
1960, MOSFET, D. Kahng and M. Atalla

Bell Labs

1964 - Op-Amp uA702, Fairchild

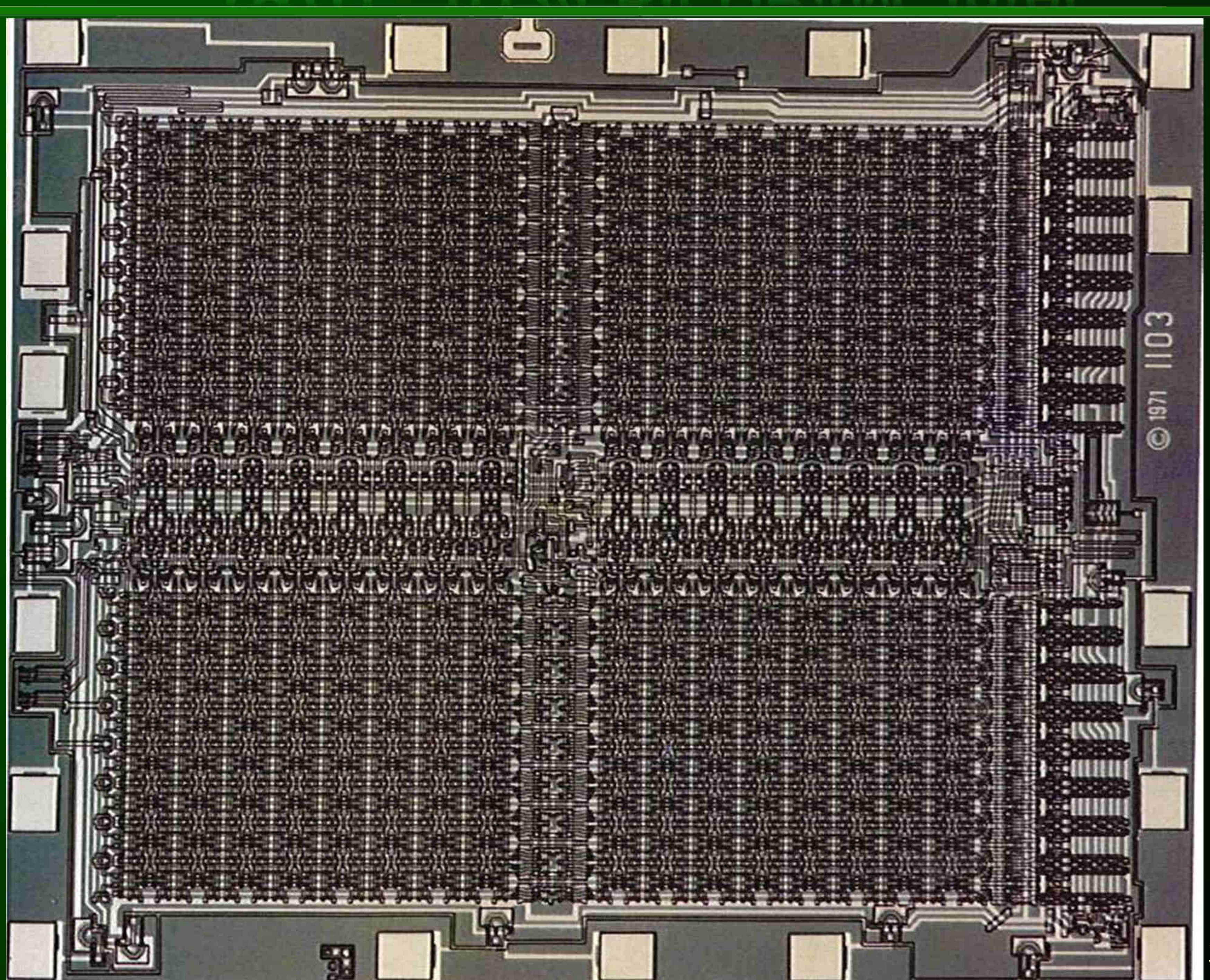


1965 - Op-Amp uA709, Fairchild

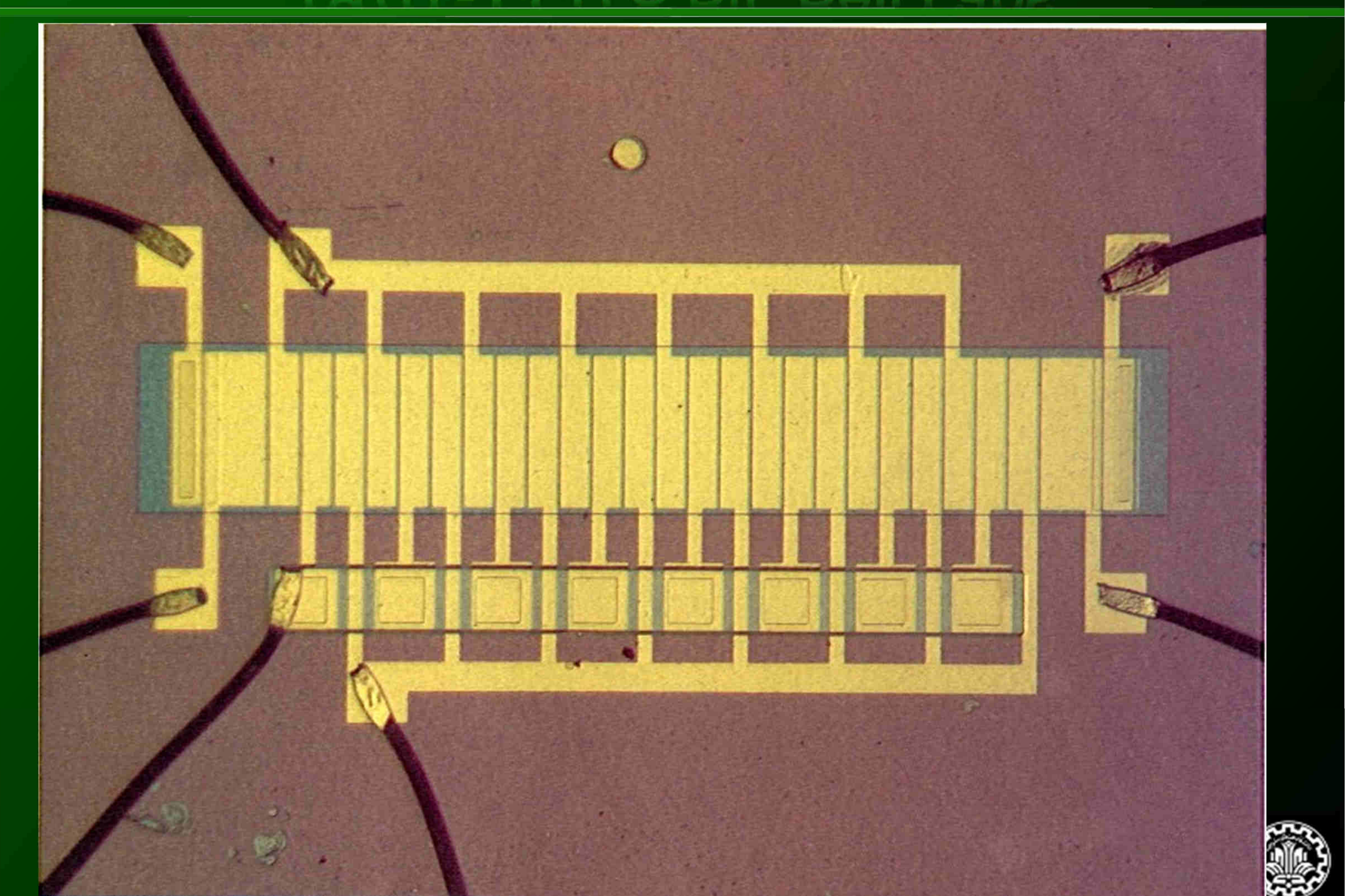


1970 - SRAM 256 Bit, Fairchild

1970 - 1024 Bit DRAM, Intel

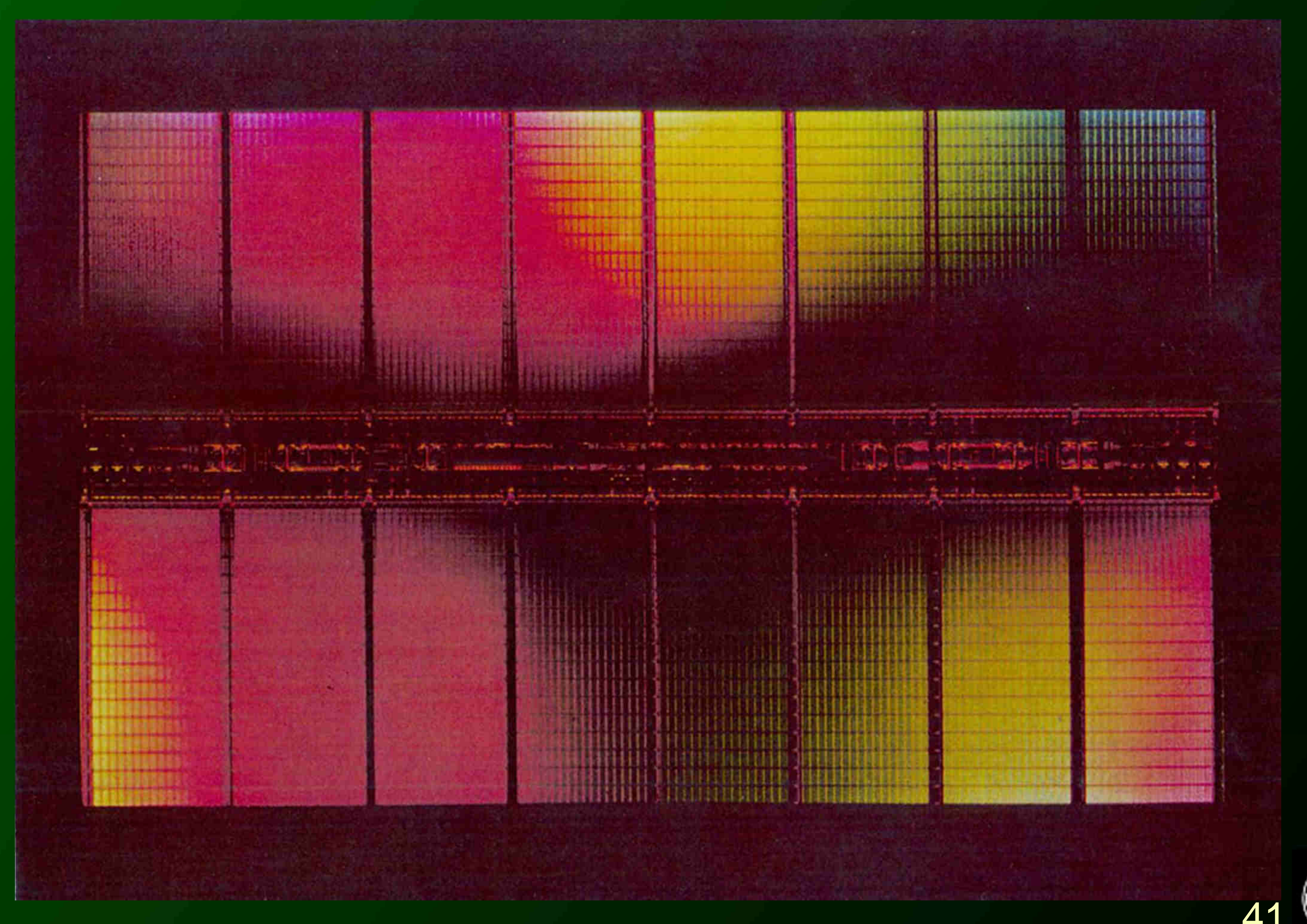


1970 - CCD 8 Bit, Bell Labs

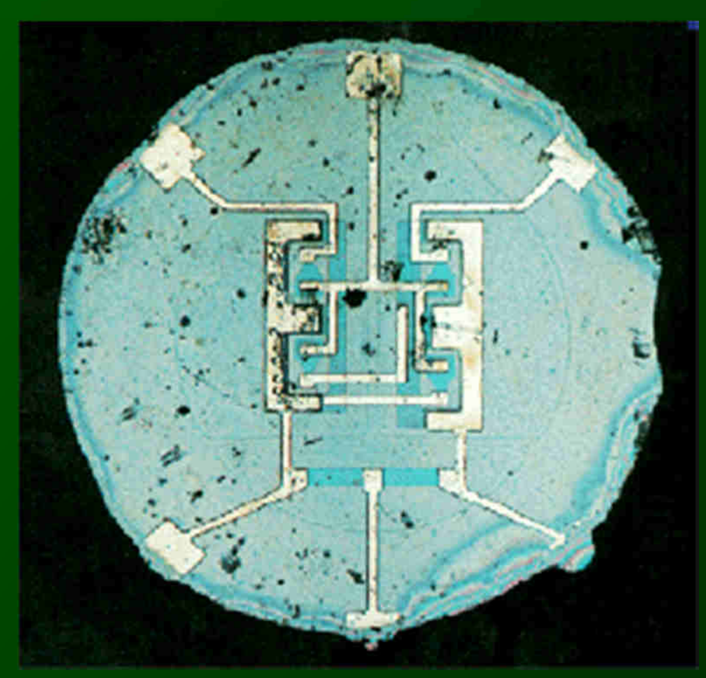


1971 - Microprocessador 4004, Intel

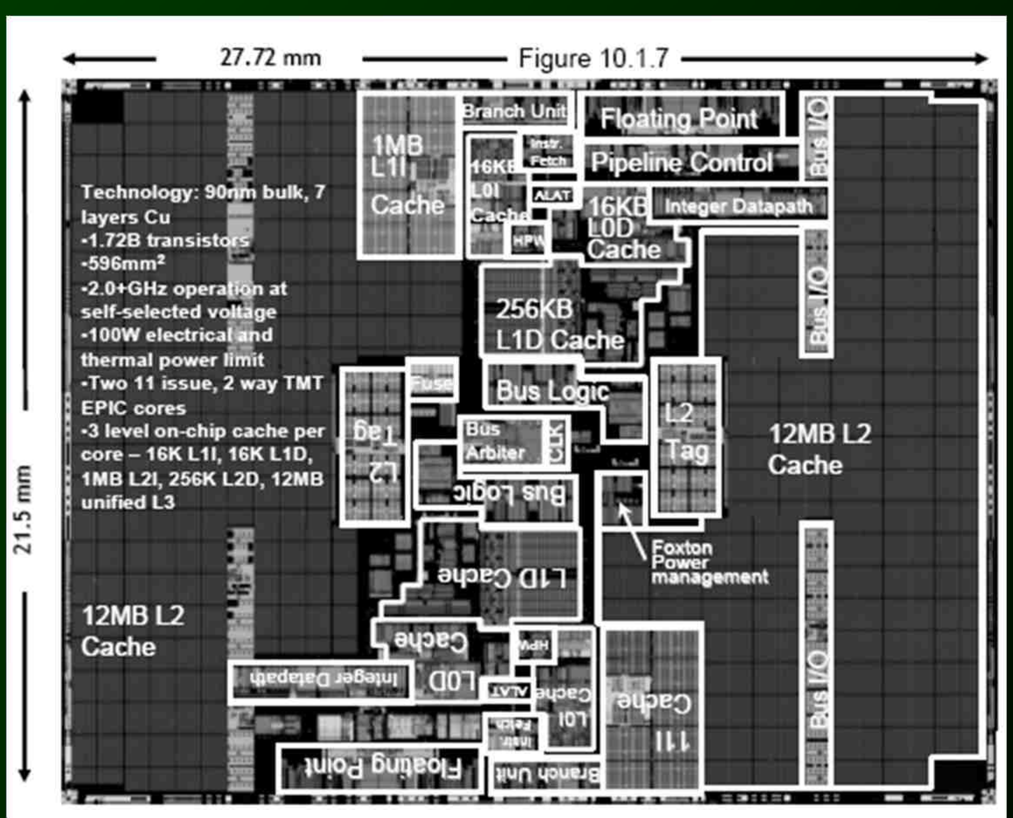
2001 - 256Mbit DRAM , TOSHIBA



Circuits: from 1961 to 2005

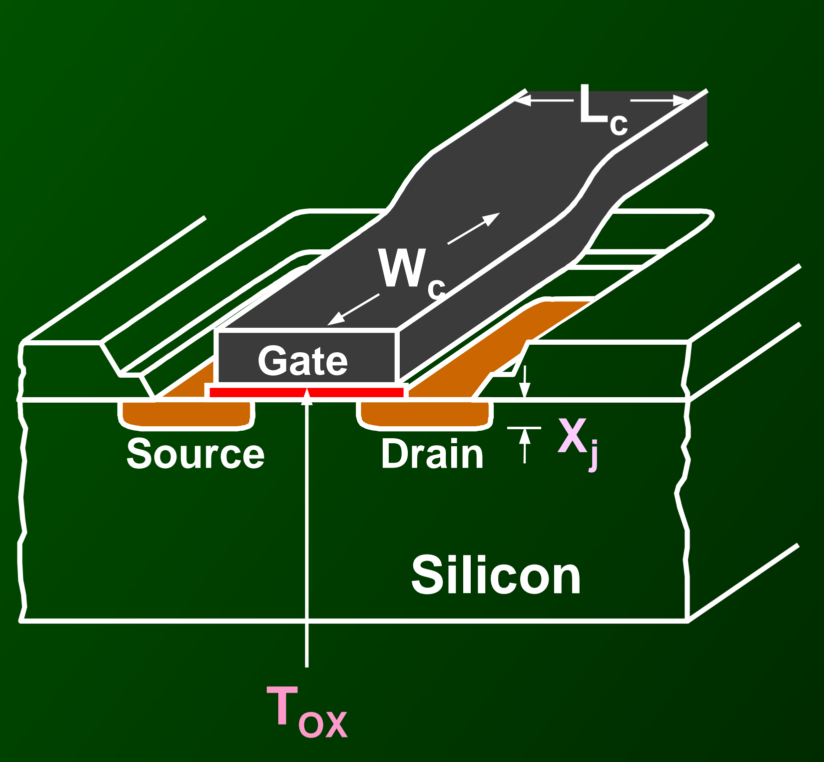


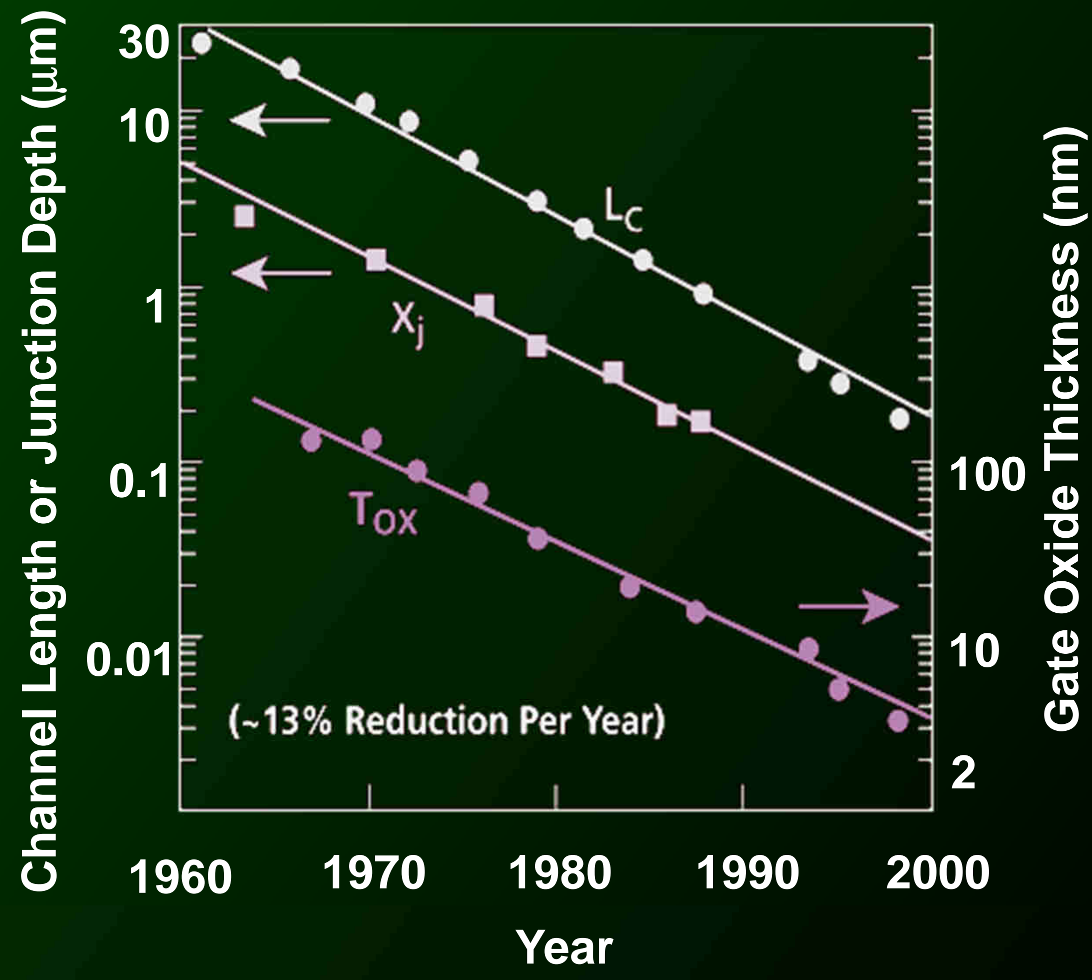
The first planar integrated circuit, 1960.
Designed and built by Lionel Kattner and Isy Haas under the direction of Jay Last at Fairchild Semiconductor.



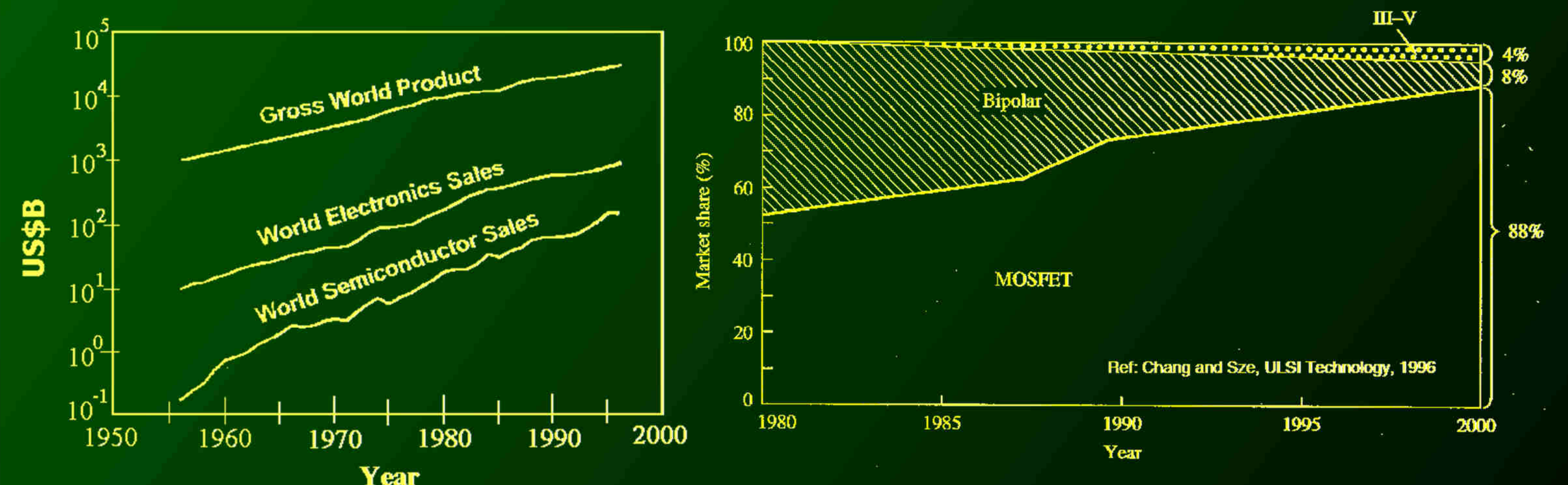
The Intel "Montecito" microprocessor, 2005

Scaling of MOSFET Dimensions





Trends in Semiconductor/CMOS Market



Semiconductors have become increasingly more important part of world economy

In 2000: 0.7% of GWP
Today: 5% of GWP

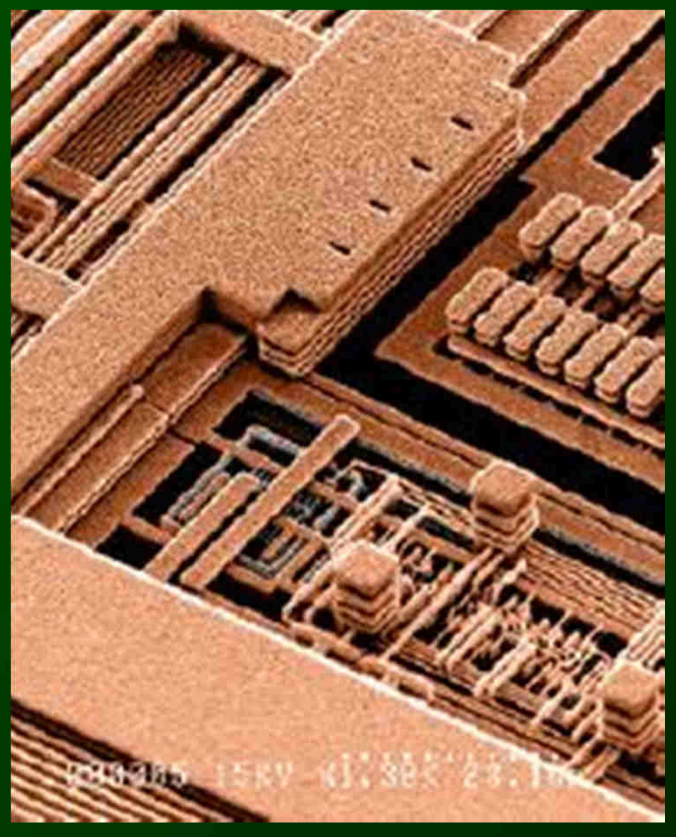
CMOS has become the pervasive technology

Interconnect?!

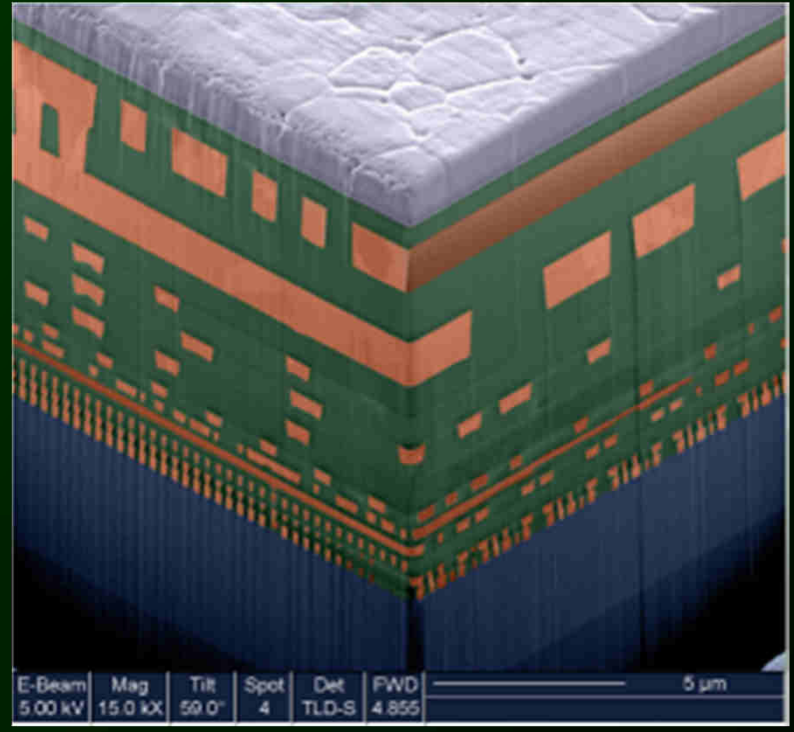
2 Major problems facing Moore's law:

- Power dissipation
- Interconnects

IBM Cu technology



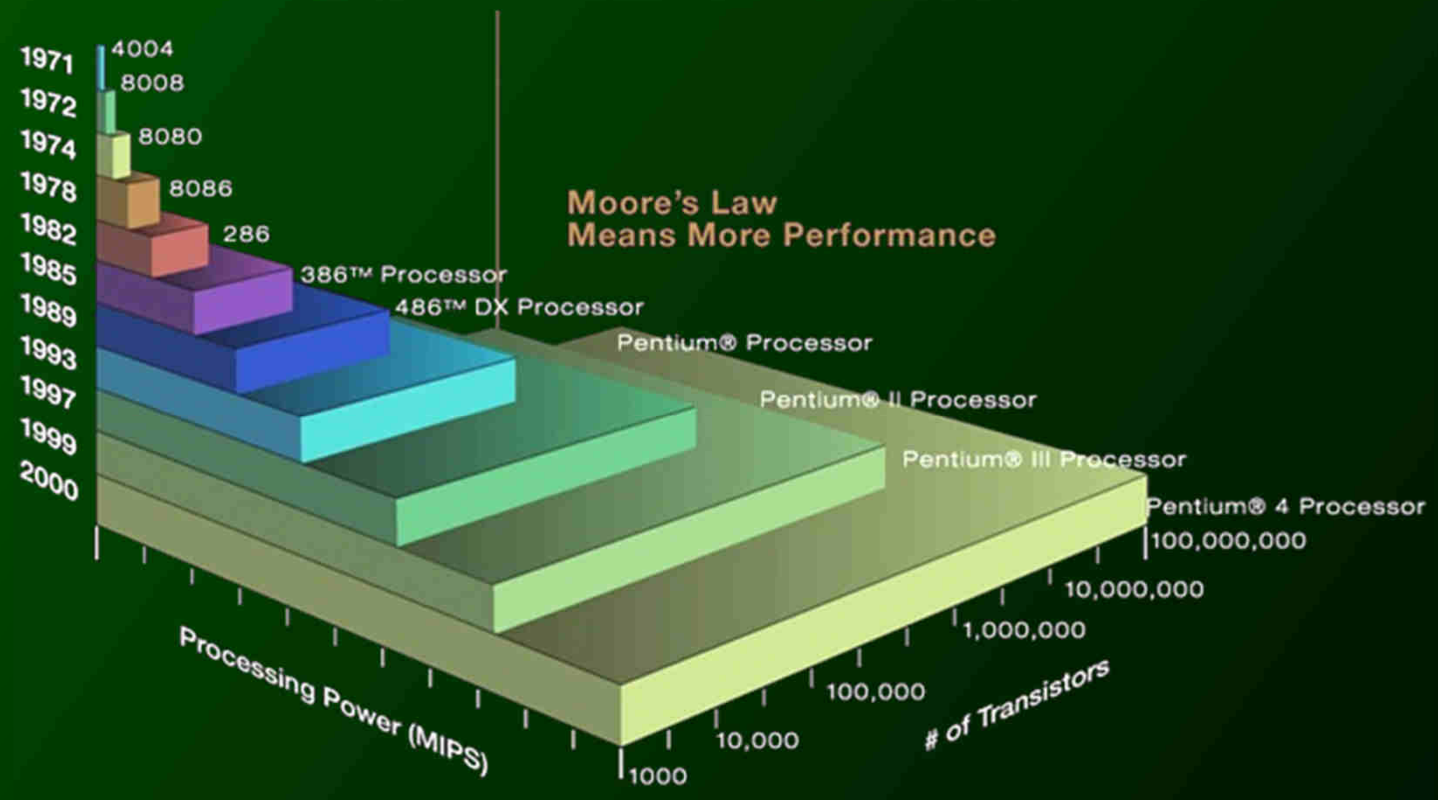
from IBM
Cross-section of 64-bit high-performance microprocessor



Connectivity and Complexity

Challenge of System Complexity

Moore's Law



Moore's Law, the empirical observation that the transistor density of integrated circuits doubles every 2 years.

Moore: Moore's law has been the name given to everything that changes exponentially. I say, if Gore invented the Internet, I invented the exponential.

Moore's Law in Perspective

The number of transistors shipped in 2003 had reached about 10^{18}. That's about 100 times the number of ants estimated to be in the world.

A chip-making tool levitated images within a tolerance of 1/10,000 the thickness of a human hair — a feat equivalent to driving a car straight for 1000 km while deviating less than one 3.8cm.

It would take you about 25,000 years to turn a light switch on and off 1.5 trillion times, but Intel has developed transistors that can switch on and off that many times each second..

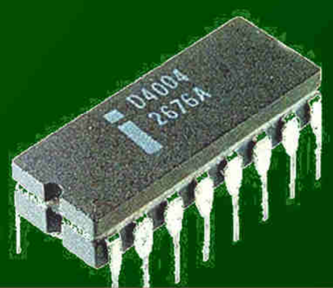
Moore's Law in Perspective

In 1978, a flight between New York and Paris cost around $900 and took 7 hours. If the principles of Moore's Law had been applied to the airline industry the way they have to the semiconductor industry, that flight would now cost about a penny and take less than 1 sec.

The price of a transistor is now about the same as that of one printed newspaper character.

Intel has developed transistors so small that about 200 million of them could fit on the head of each of these pins.

Intel µP Trends



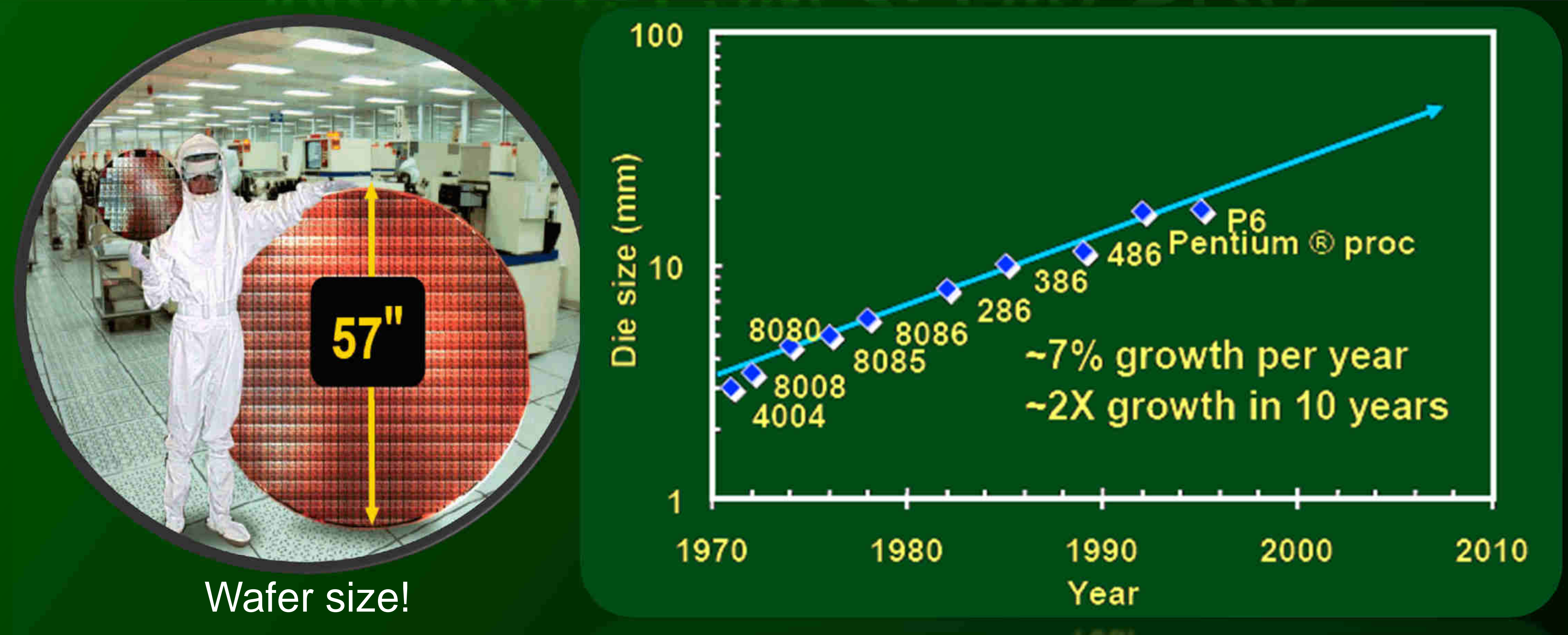
- Intel 4004: first single-chip microprocessor

- November 15, 1971
- Clock rate 740 kHz
- Bus Width 4 bits (multiplexed address/data due to limited pins)
- PMOS
- 2,300 Transistors at **10 µm**
- Addressable Memory 640 bytes
- Program Memory 4 KB (4 KB)

- Intel Core i7

- Today
- Clock rate 2.66GHz-3.33GHz
- 64 bit processor
- 4 cores
- 731M Transistors at **45 nm**
- Oregon 32 nm plant
- Price 273-562 $
- 263 mm2 die size

Moore's Law & Die Size



Wafer size!

Moore was not always accurate

Projected Wafer in 2000, circa 1975

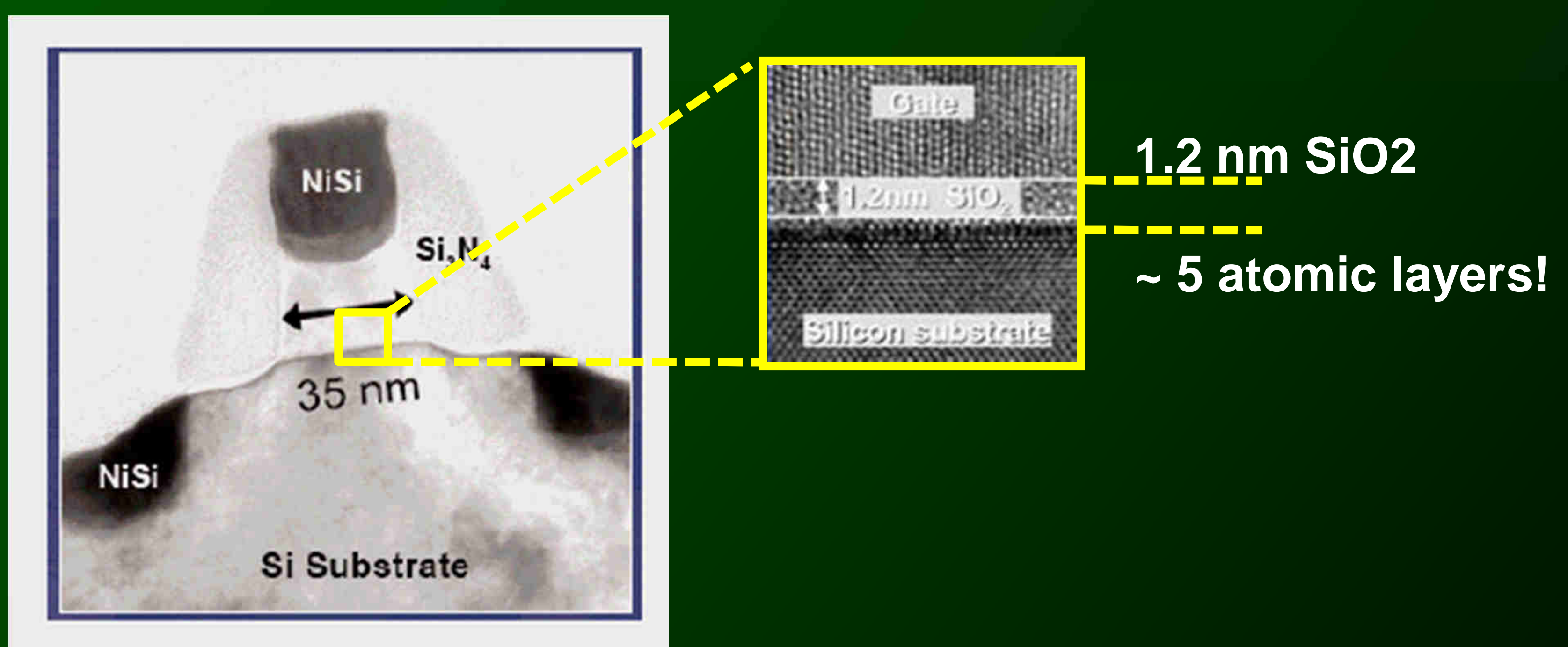
Die size has grown by 14% to satisfy Moor's law, BUT the growth is almost stopped because of manufacturing and cost issues

The die size of the processor refers to its physical surface area size on the wafer, the first generation Pentium used a 0.8 micron circuit size, and required 296 mm^2 per chip. The second generation chip had the circuit size reduced to 0.6 microns, and the die size dropped by a full 50% to 148 mm^2!!!

Trends in Clock Frequency

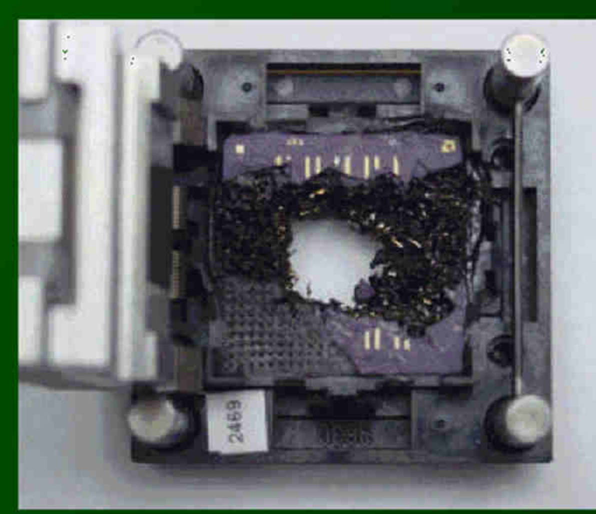
Lead microprocessors frequency doubles every 2 year, BUT the growth is slower because of power dissipation issue

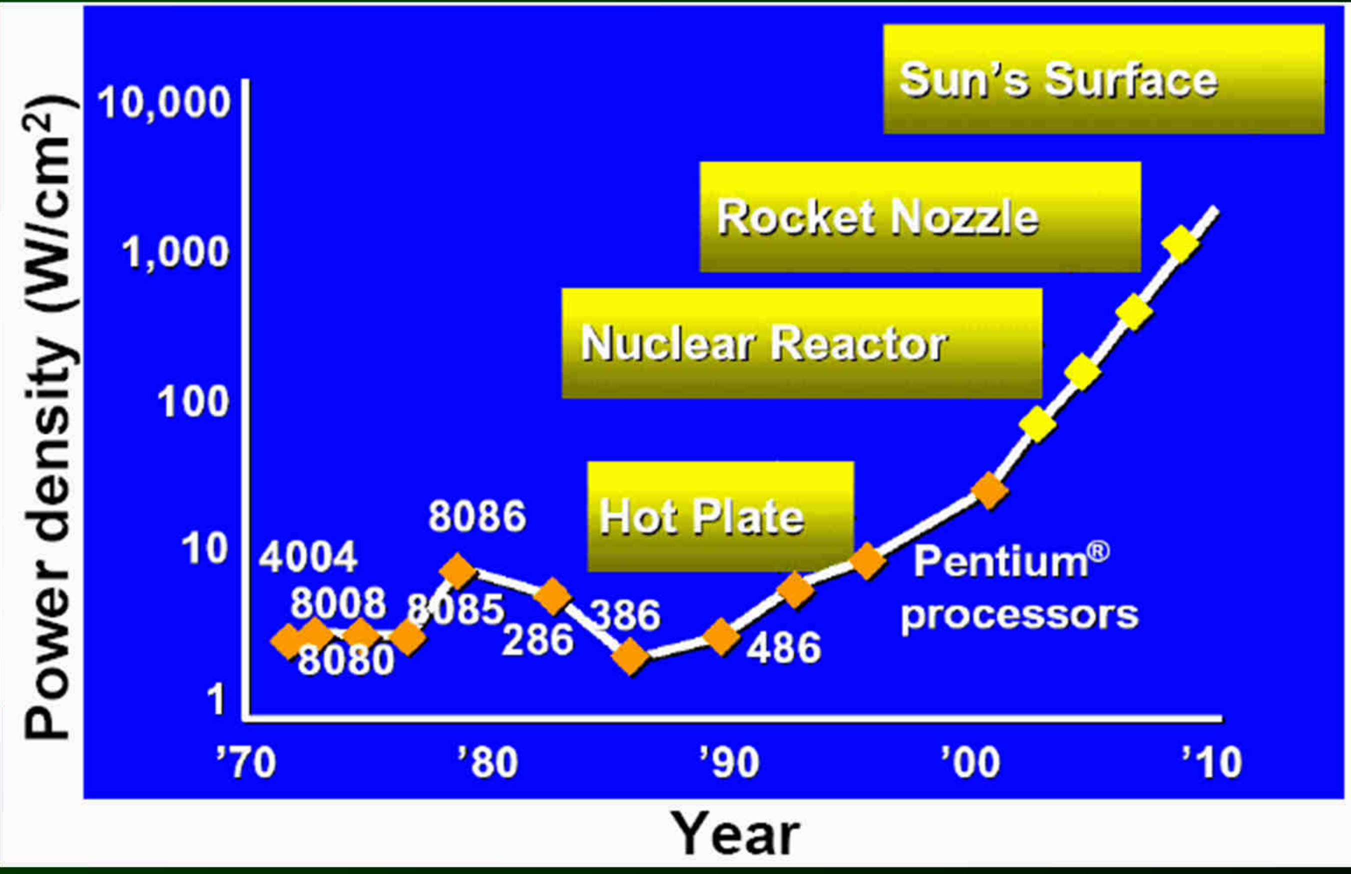
Gate Insulator Thickness in 65nm



Problem: Electrons can easily jump over
the 5 atomic layers!
This is known as leakage current

Power Density Problem





Power density too high to keep junction at low temperature.
Power reaching limits of air cooling.

Power Density Problem

Power = 115 Watts
Supply Voltage = 1.2 V
Supply Current = 115 W / 1.2 V
= 96 Amps!

Note:
Fuses used for household appliances = 15 to 40 Amps

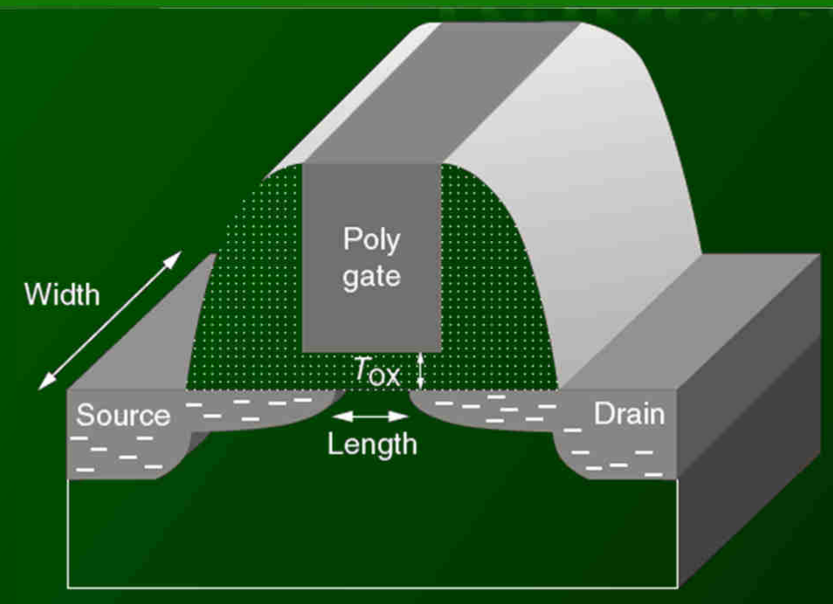
Problem:
Current density becomes a serious problem!
This is known as electromigration

Power = 115 Watts
Chip Area = 2.2 cm^2
Heat Flux = 115 W / 2.2 cm^2
= 50 W/cm^2 !

Notes:
Heat flux in iron = 0.2 W/cm^2
Heat flux in frying pan = 10 W/cm^2

Problem:
Heat flux is another serious issue!

Transistor Scaling



$$T_{Delay} = C_{Gate} \frac{V_{DD}}{I_{Drive}}$$

$$= \frac{WL}{T_{ox}} \frac{V_{DD}}{I_{Drive}}$$

$$I_{Drive} = \frac{W}{LT_{ox}} \cdot (V_{DD} - V_{Th})^2$$

$$T_{Delay} = L^2 \frac{V_{DD}}{(V_{DD} - V_{Th})^2}$$

Scaling Issues:

- Channel length modulation
- Drain induced barrier lowering
- Punch through
- Sub-threshold current
- Field dependent mobility / Velocity saturation
- Avalanche breakdown and parasitic bipolar action
- Oxide Breakdown
- Interconnect capacitance
- Heat production
- Process variations
- Modeling challenges

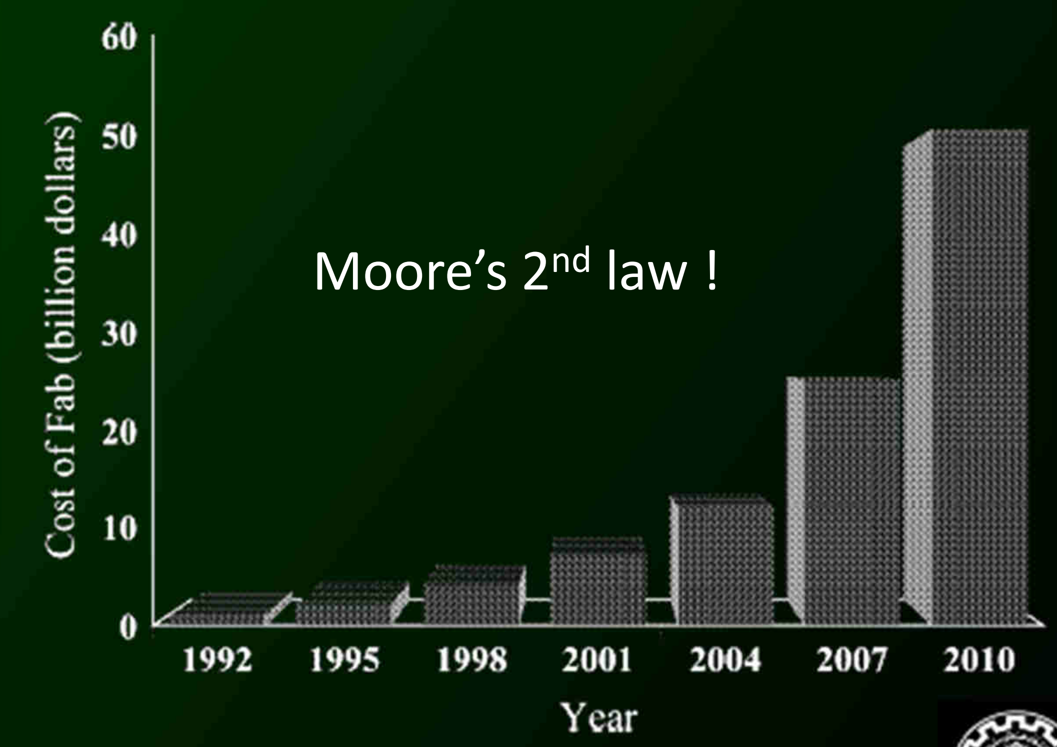
Limit of "Moore's Law"?

- What is behind this fantastic race of development of the IC technologies?
  - Is it the "technological" will and motivation of the people involved?
  - Or/and is it the economical drive the main force?
  - Semiconductor industry sales:
    - 1962, > $1-billion
    - 1978, > $10-billion
    - 1994, > $100-billion

a law of human ingenuity, not of nature

2 prominent technical: (DRAM), uP

Will physics or economics stop Moore's law ?



Physical limits to computation

The min. energy perform a logic operation in time Δt

$$E \geq \pi\hbar/2\Delta t$$

$\hbar = 1.0545 \times 10^{-34}$ J.s

max # of operations per second $N = 2E/\pi\hbar$

Entropy $S = k_B \ln W$ # of states

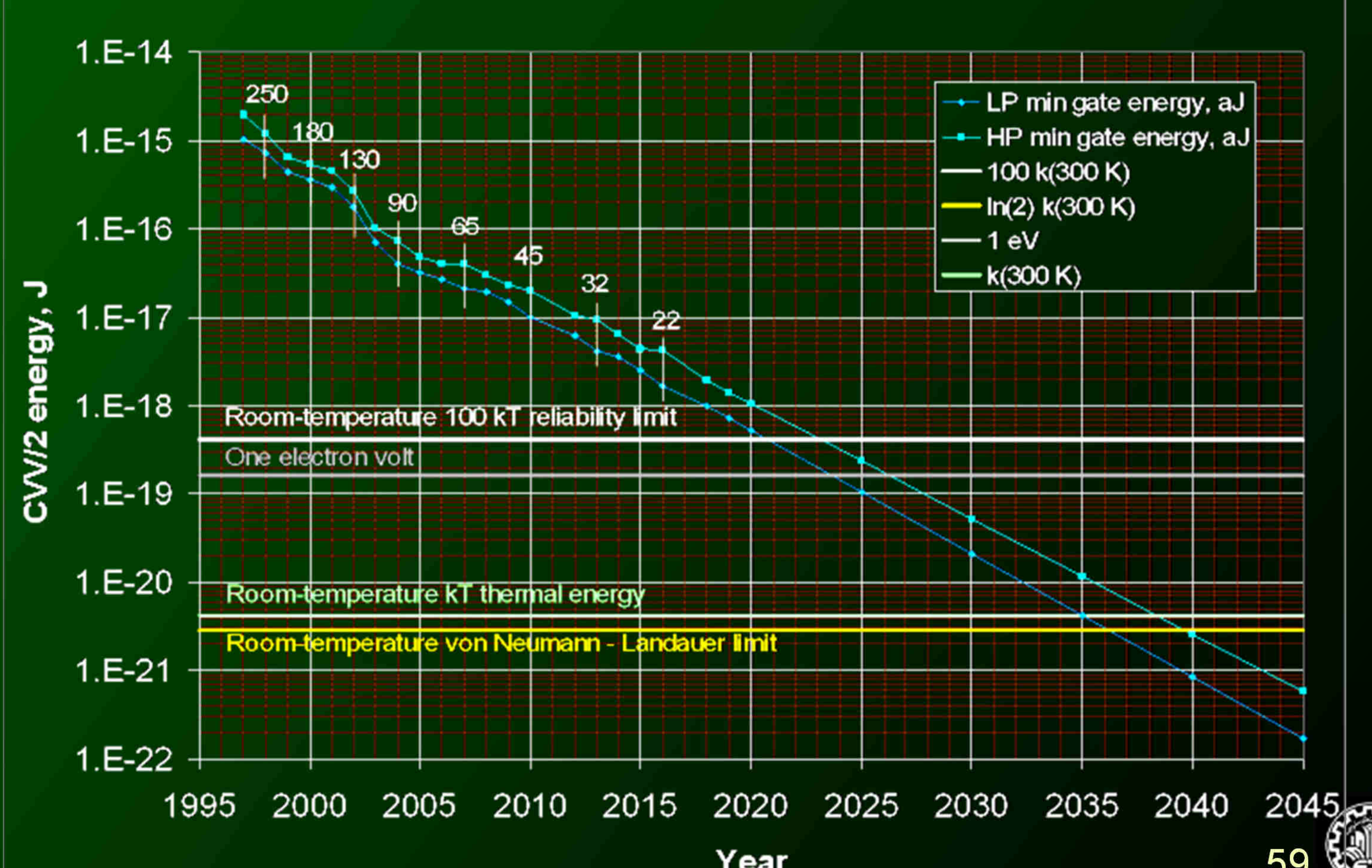
$k_B = 1.3805 \times 10^{-23}$ J/K

# of bits $m = S/k_B \ln 2$

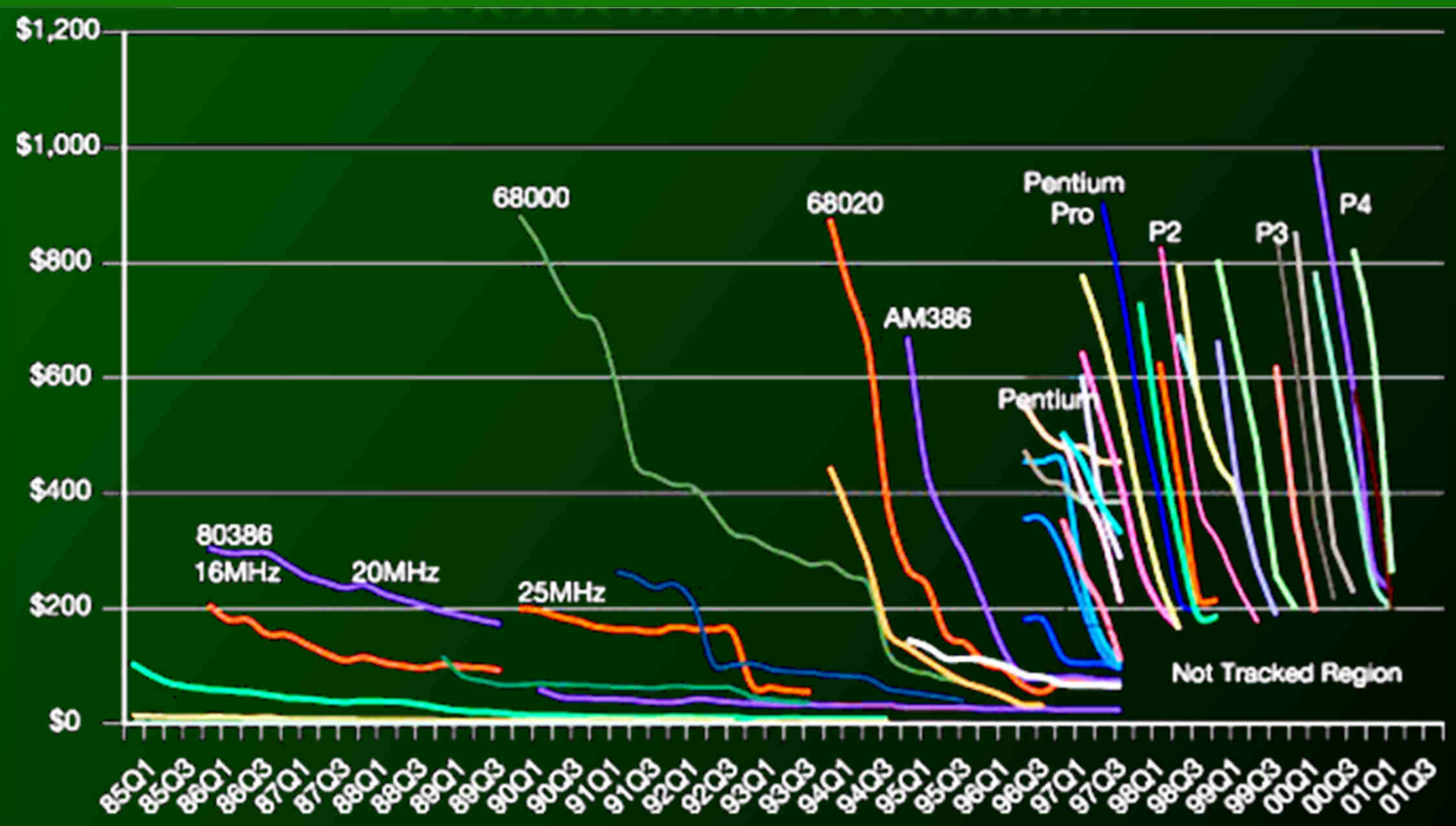
$$\frac{\text{operation}}{\text{bit . sec}} = \frac{N}{m} = \frac{2Ek_B \ln 2}{\pi\hbar S} \sim \frac{2k_B T \ln 2}{\pi\hbar}$$

minimal amount of energy required to 1 bit : $\sim k_B T \ln 2$

Min. Transistor Switching Energy



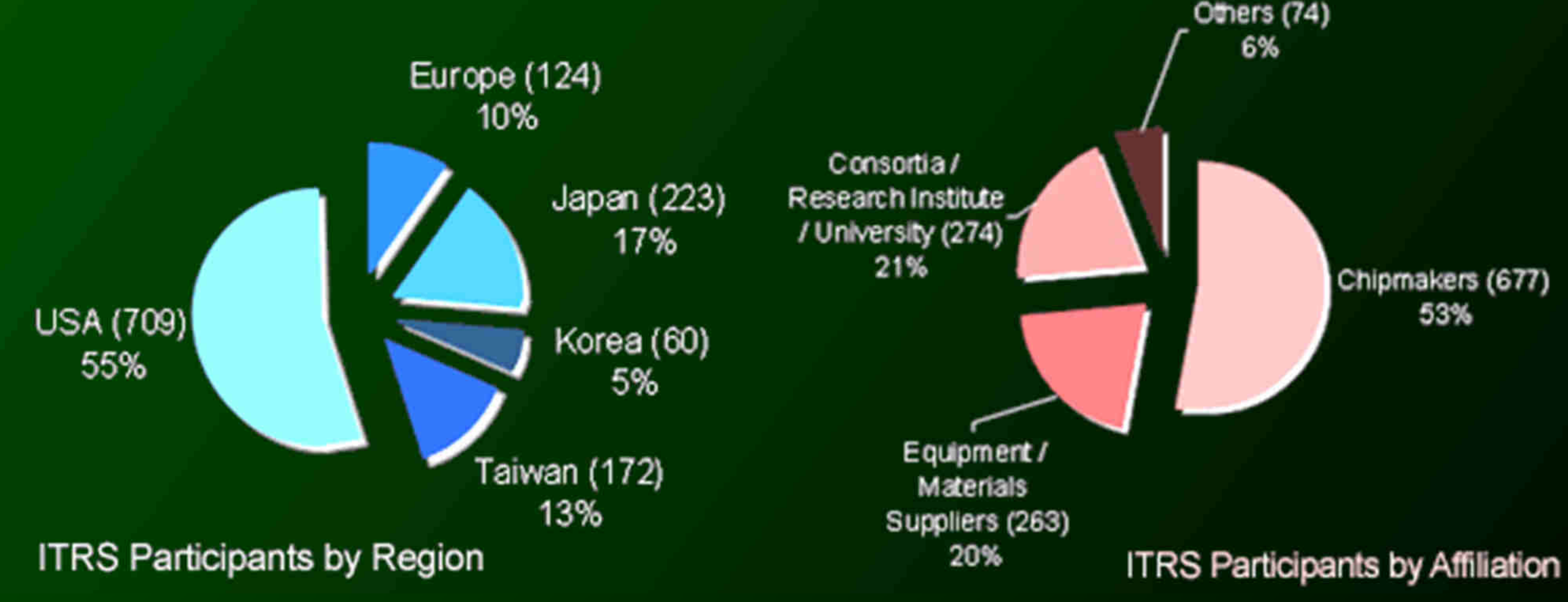
Economic trends



Product lifecycles and the products selling prices
are decreasing at an increasing rate.
(Based on information from DataQuest and MicroDesign Resources)

ITRS

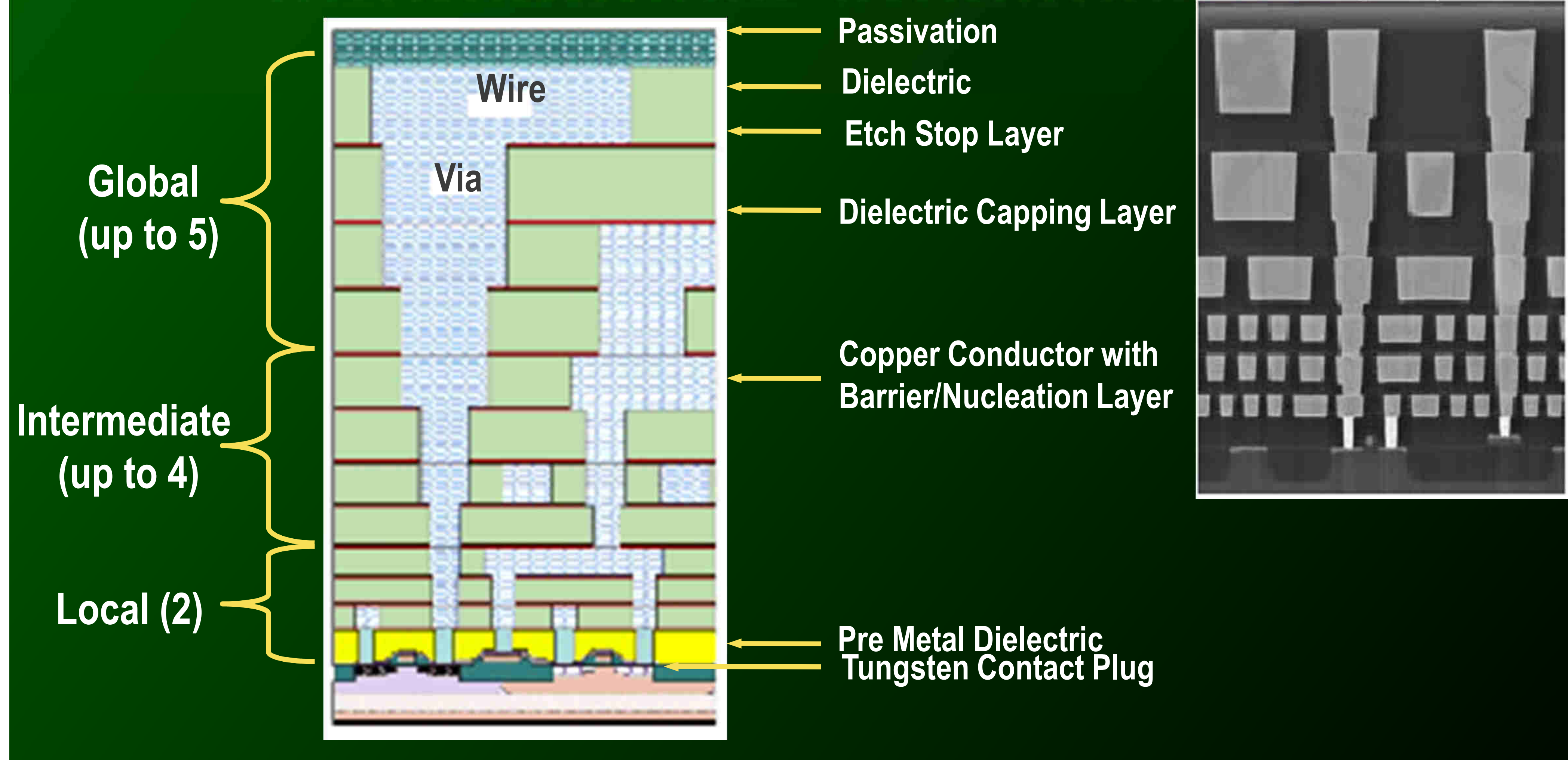
The International Technology Roadmap for Semiconductors is sponsored by the five leading chip manufacturing regions in the world: Europe, Japan, Korea, Taiwan, and the United States



http://www.itrs.net/reports.html

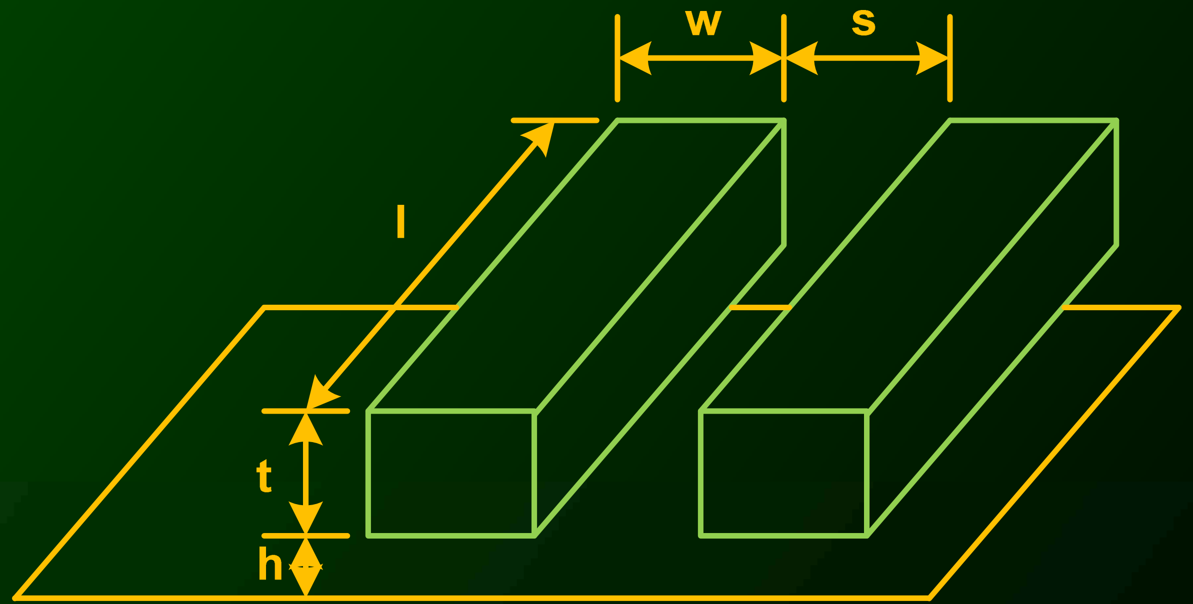
“Prediction is very difficult, especially if it's about the future”
Niels Bohr

Interconnect Architecture



Wire Geometry

- Pitch = w + s
- Aspect ratio: AR = t/w
  - Old processes had AR << 1
  - Modern processes have AR ≈ 2
  - Pack in many skinny wires



ITRS Interconnect Technology Requirement

Short Term

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Number of metal levels	11	11	11	12	12	12	12	12	13
Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4	4	4
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	1019	1212	1439	1712	2000	2222	2500	2857	3125
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	4.9	4.1	3.5	2.9	2.5	2.3	2	1.8	1.6
J_{max} (A/cm^2) – intermediate wire (at 105°C)	8.91E+05	1.37E+06	2.08E+06	3.08E+06	3.88E+06	5.15E+06	6.18E+06	6.46E+06	8.08E+06
Metal 1 wiring pitch (nm)	180	156	136	118	104	90	80	72	64
Metal 1 A/R (for Cu)	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9

Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (◆)
Manufacturable solutions are NOT known (red)

ITRS Interconnect Technology Requirement

Long Term

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal levels	**13**	**13**	**13**	**14**	**14**	**14**	**14**
Number of optional levels – ground planes/capacitors	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	**3571**	**4000**	**4545**	**5000**	**5555**	**6250**	**7143**
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	**1.4**	**1.3**	**1.1**	**1**	**0.9**	**0.8**	**0.7**
J_{max} (A/cm^2) – intermediate wire (at 105°C)	**1.06E+07**	**1.14E+07**	**1.47E+07**	**1.54E+07**	**1.80E+07**	**2.23E+07**	**2.74E+07**
Metal 1 wiring pitch (nm)	**56**	**50**	**44**	**40**	**36**	**32**	**28**
Metal 1 A/R (for Cu)	**1.9**	**1.9**	**2**	**2**	**2**	**2**	**2**

Manufacturable solutions exist, and are being optimized (white)
Manufacturable solutions are known (yellow)
Interim solutions are known (yellow with red diamond)
Manufacturable solutions are NOT known (red)

VLSI Industry

semiconductor industry(2006): revenues of ~200 billion US $ annually

Computer:
Volatile Memories

static random access memory (SRAM)

dynamic random access memory (DRAM). They are fast but need Non

Volatile Memories:

hard disc drive (HDD). (six orders of magnitude slower than SRAM)

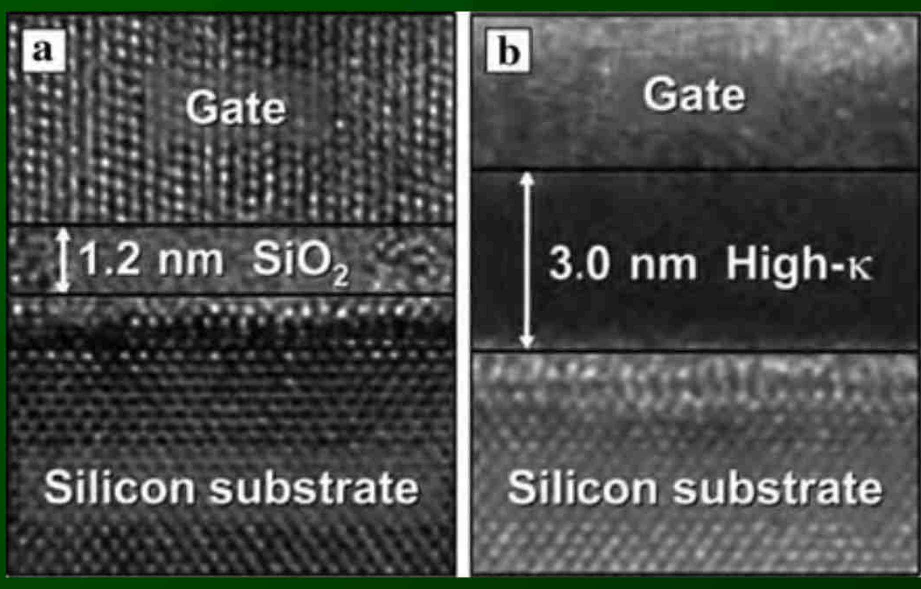
Moore's law: the density of transistors on a silicon-based integrated circuit (IC), and so the attainable computing power, doubles about every 18 months,

	1980	2007
time	2 day	10ms
x		20,000,000
Hardware x		4,000

Moore's Law!

	1999 180nm	2001 130nm	2003 90nm	2005 65nm	2007 45nm	2009 20nm	2011 10nm
Transistor					30 nm	20 nm, 40 nm, L_G=20nm	10 nm
Interconnect							
	L_G=100nm $CoSi_2$ 6 Al SiOF	L_G=70nm $CoSi_2$ 6 Cu SiOF	L_G=50nm NiSi Strain Si 7 Cu Low-k	L_G=35nm NiSi 2D Strain 8 Cu Low-k	L_G=30nm	L_G=20nm	L_G=10nm

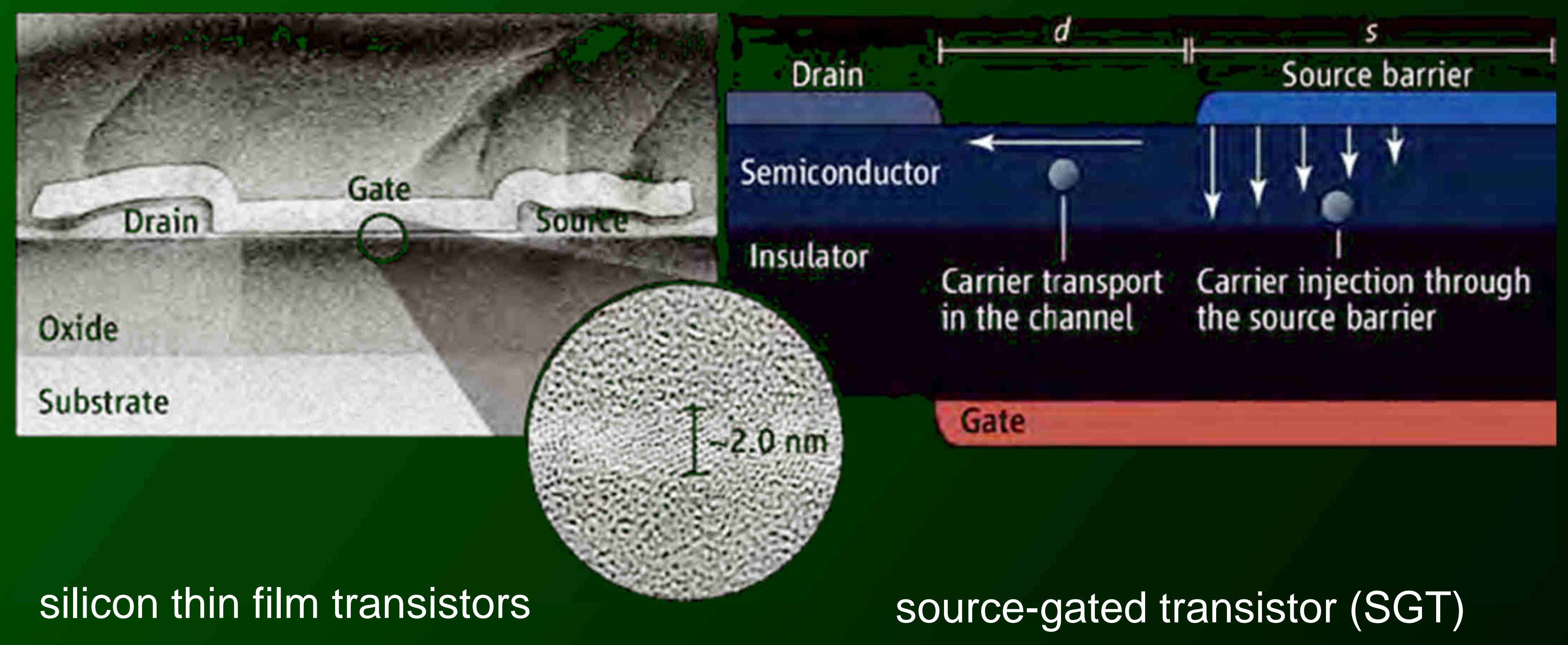
Gate Tunneling



60% bigger capacitance

100x reduction in gate leakage

New high-performance transistors

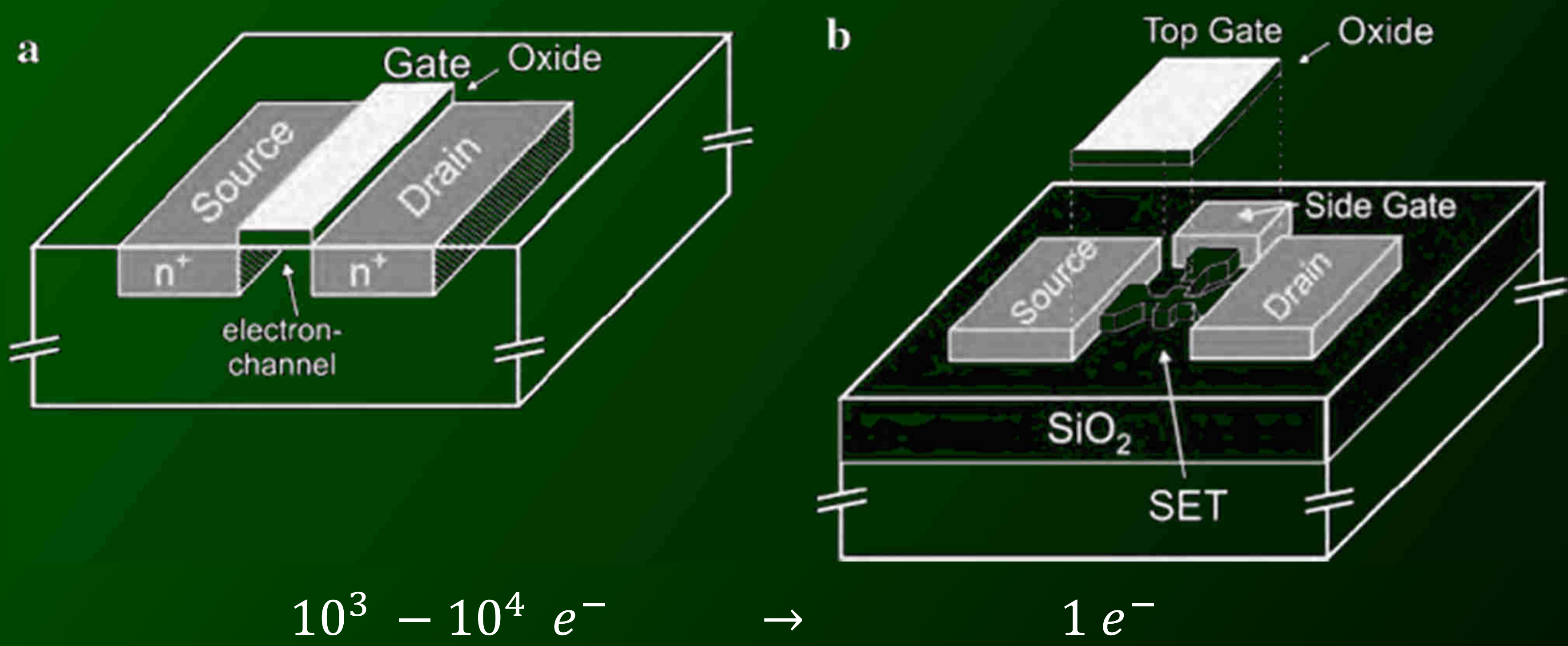


silicon thin film transistors

source-gated transistor (SGT)

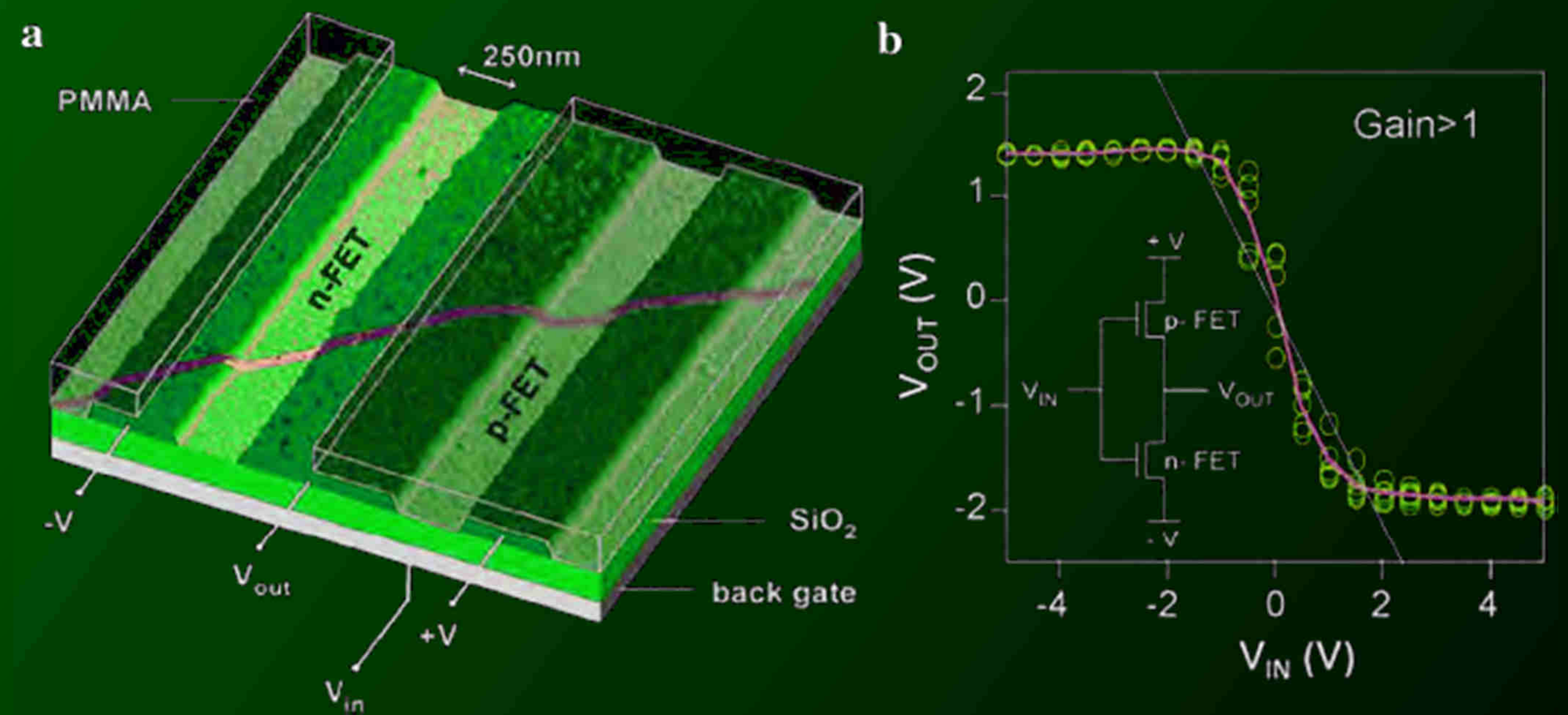
$$\frac{I_{ON}}{I_{OFF}} > 10^{11}$$

silicon-based single-electron transistor



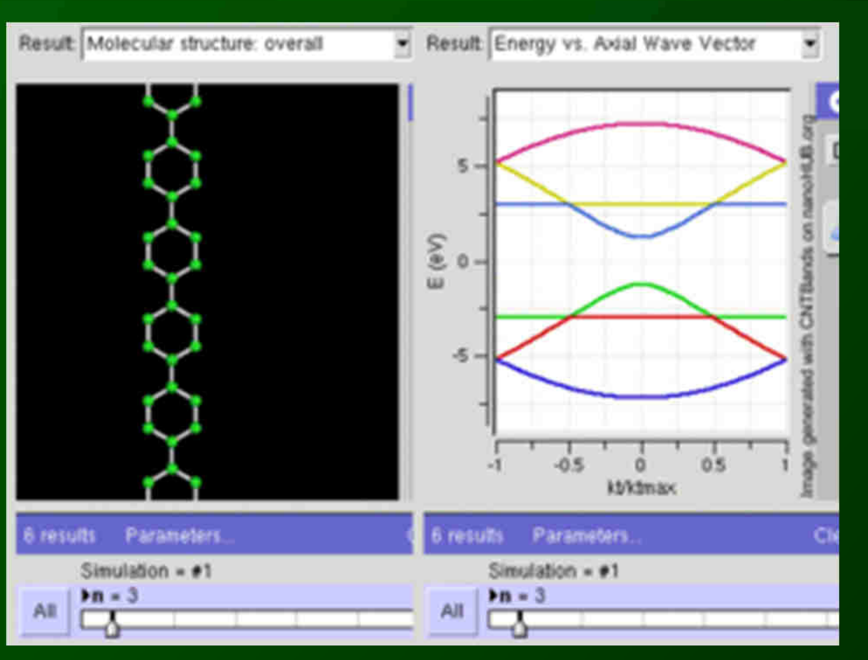
$10^3 - 10^4 \ e^- \quad \rightarrow \quad 1 \ e^-$

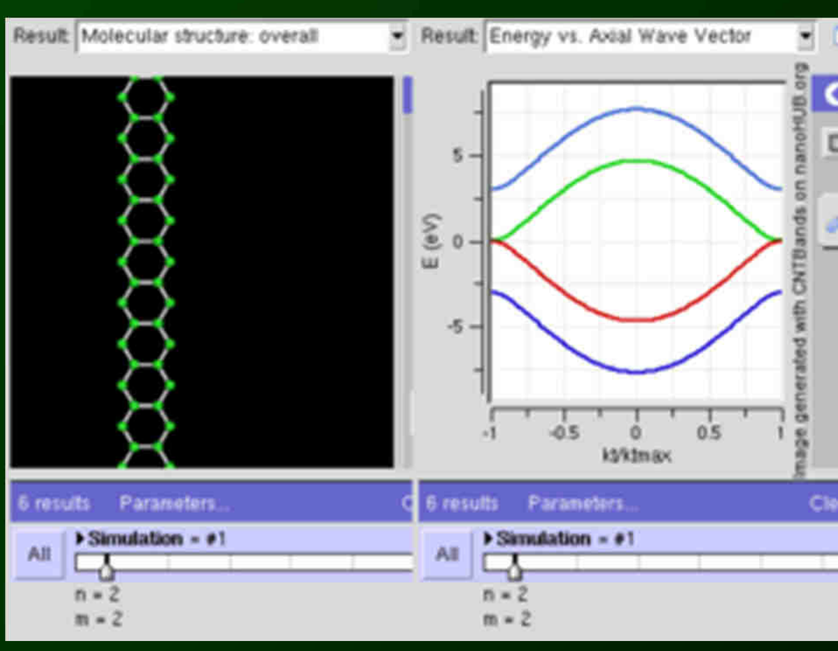
Carbon nanotube electronics

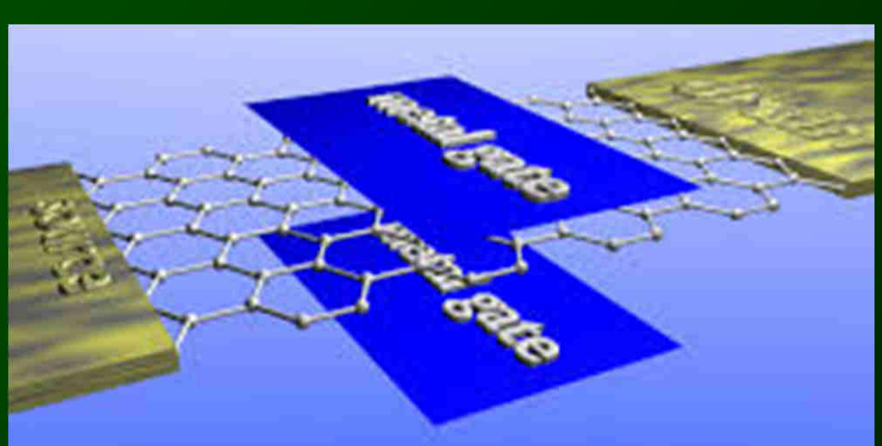


Mobility and mean free path?

Graphene NanoRibbon Field Effect Transistor







$\frac{I_{ON}}{I_{OFF}} \sim 10^6$

$I_{ON} \sim 2000\ \mu A/\mu m,$

$\mu \sim 200\ cm^2/Vs,$

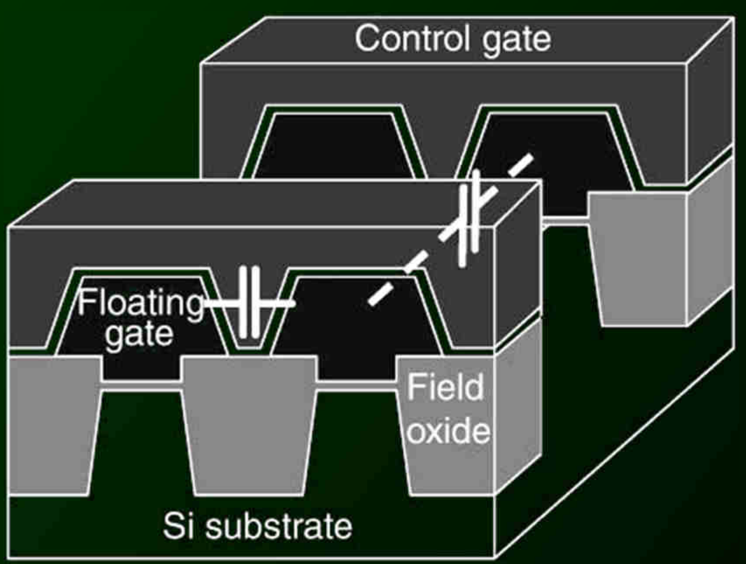
$\lambda \sim 10\ nm,$

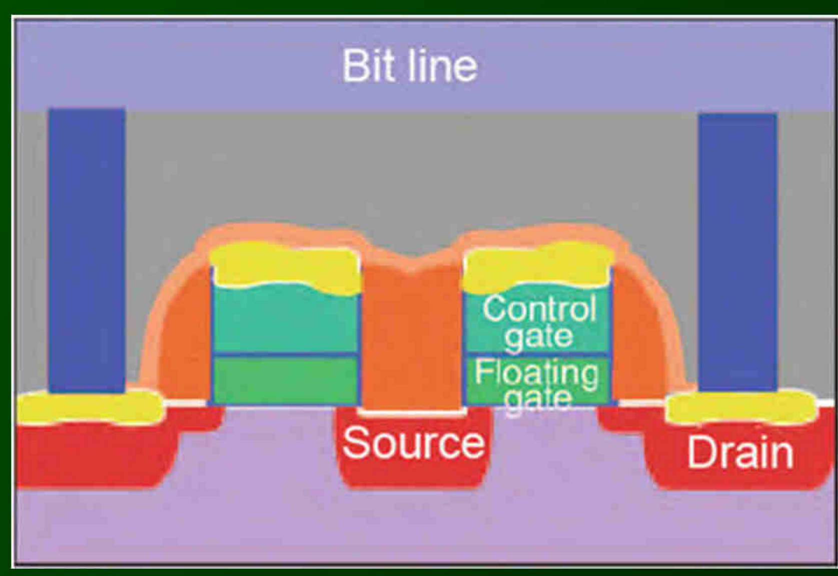
Flash Memory

invented by Dr.Fujio Masuoka in 1980 at Toshiba

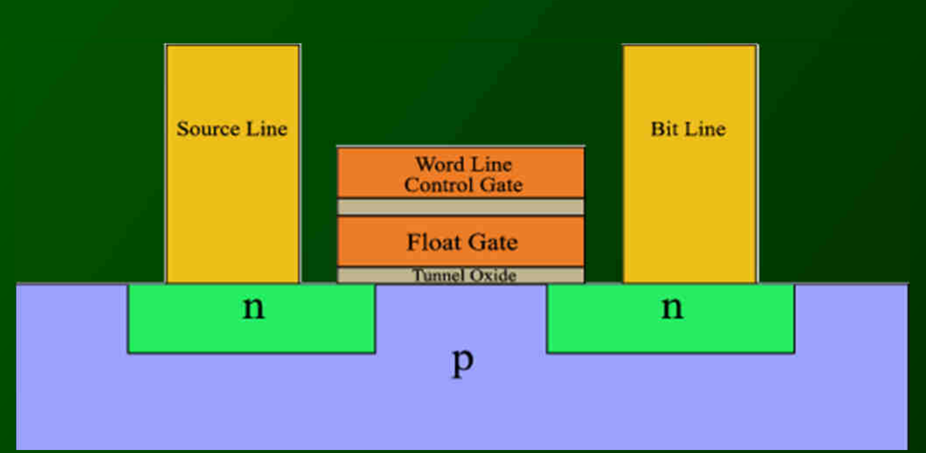
data stored in multiple memory cells to be erased in a single action (a "flash")

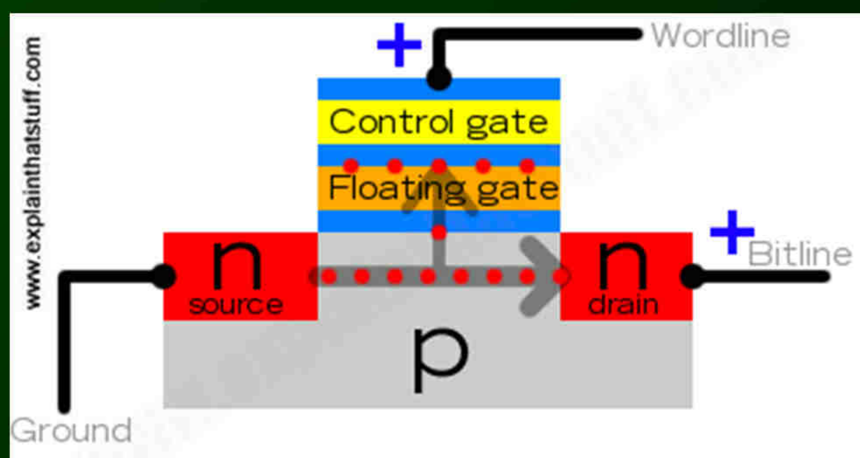
Issue: crosstalk





Flash Memory





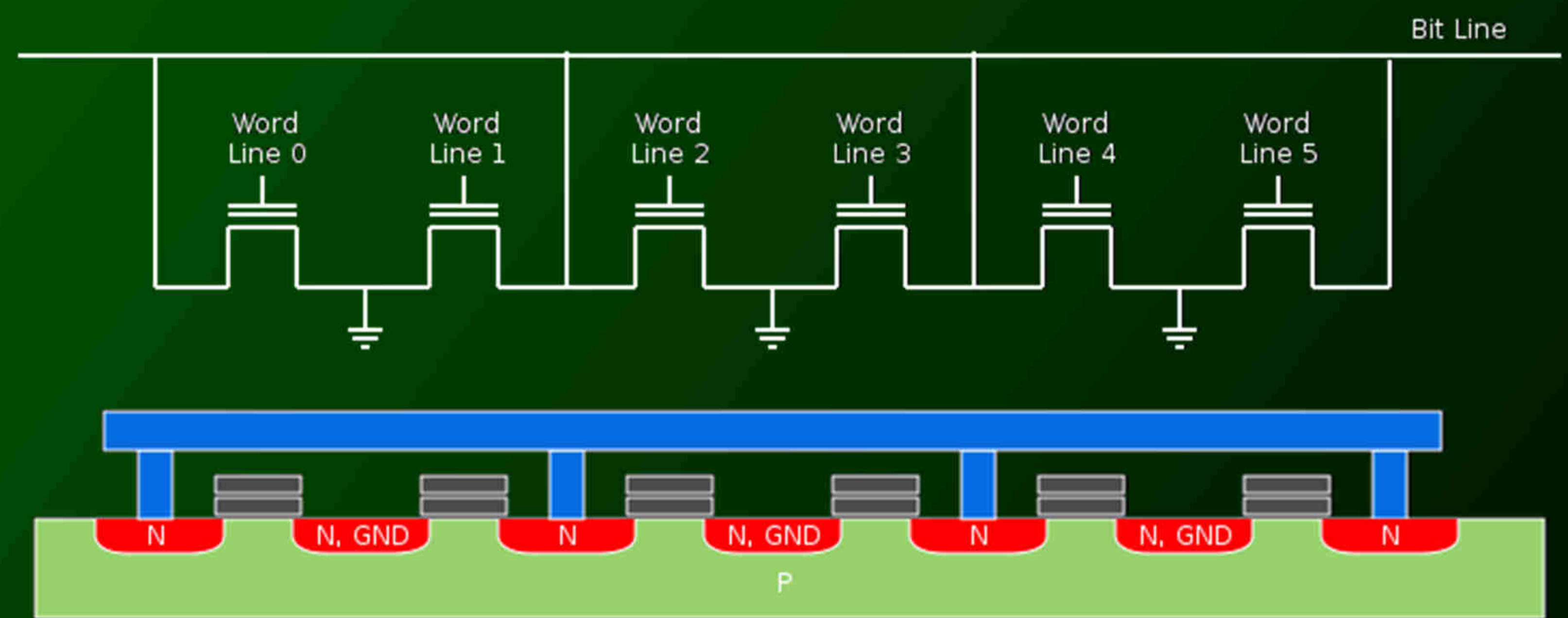
Flash is EEPROM (Electronically Erasable Programmable Read Only Memory)

You may find FLASH in:

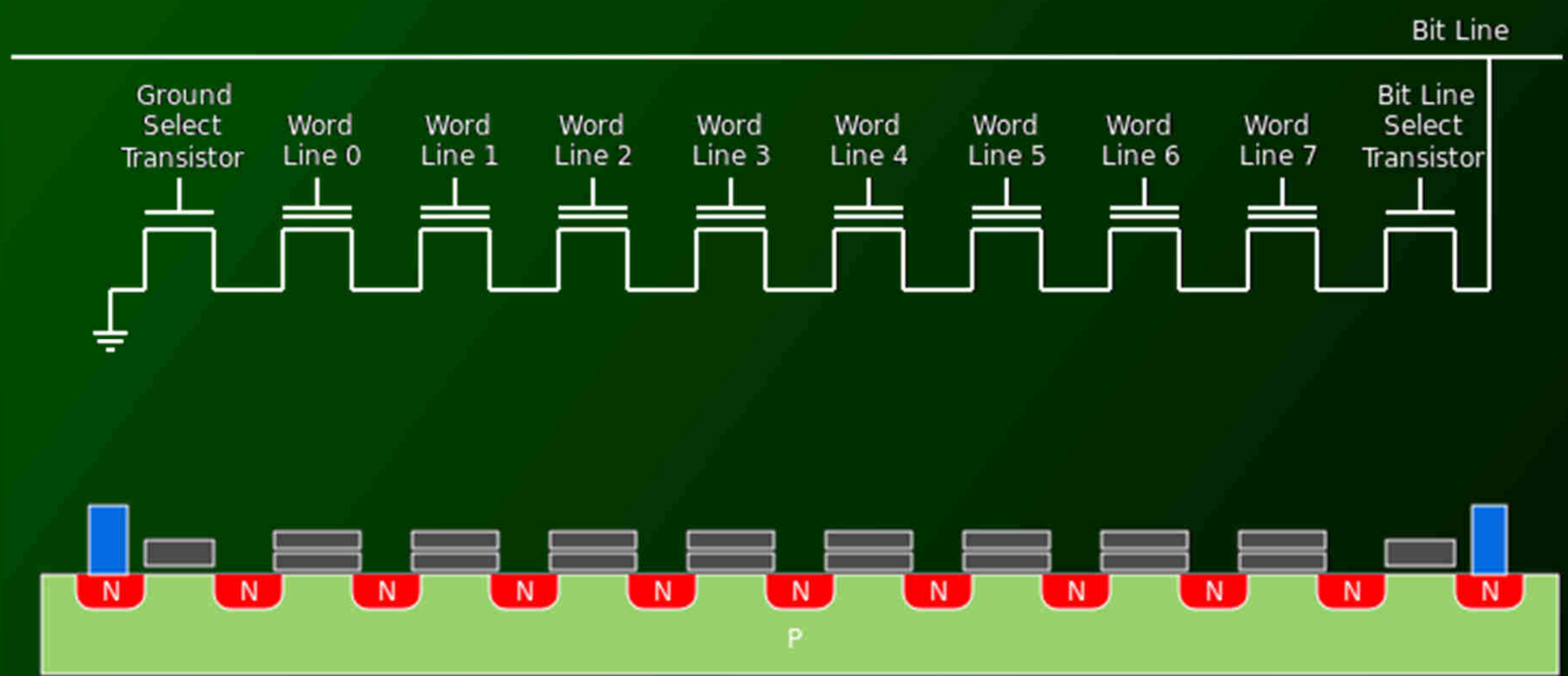
- computer's BIOS chip
- CompactFlash
- Memory Stick

NAND type is primarily used in main memory, memory cards, USB flash drives, solid-state drives (greater storage density and lower cost per bit)
The NOR type, (allows true random access) used as a replacement for the older EPROM

Flash Memory



Flash Memory



Flash Memory

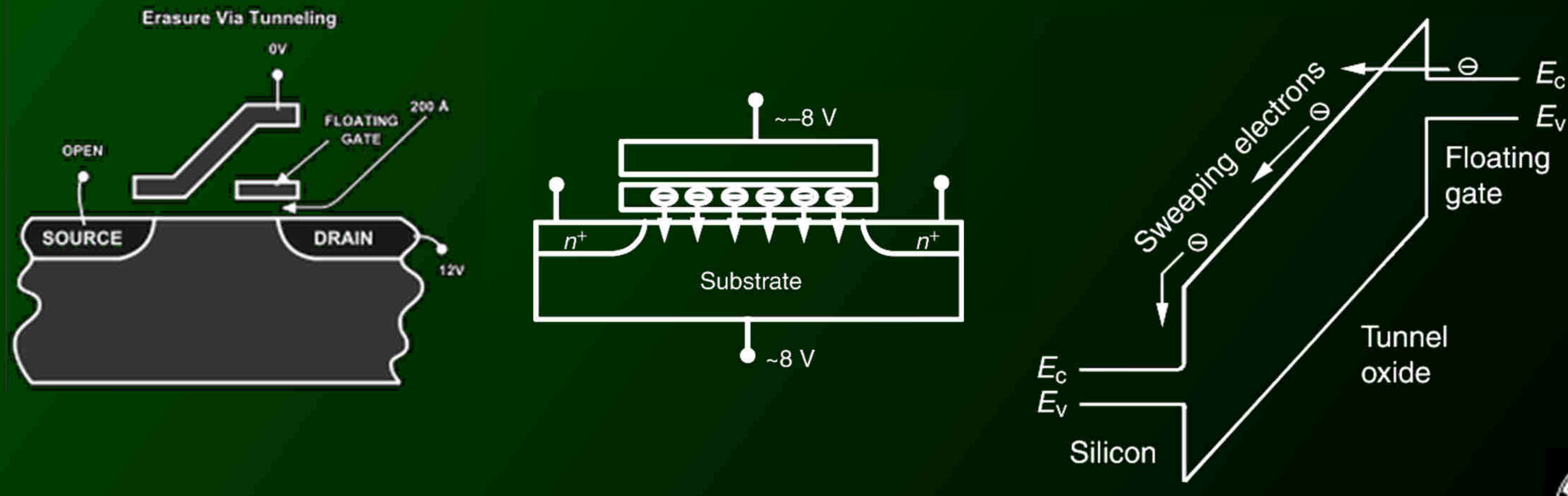
Programming a NOR memory cell (setting it to logical 0), via hot-electron injection

Programming Via Hot Electron Injection
12V
FLOATING GATE
200 Å
0V
SOURCE
DRAIN
12V

Gate ~10 V
~4 V
Source
Drain

E_c
E_v
"Lucky" electron
Substrate
Channel
E_c
E_v
Floating gate

Erasing a NOR memory cell (setting it to logical 1), via quantum tunneling



Memory Technologies

	Conventional technologies			Emerging technologies			Prototypes
Parameter	SRAM	DRAM	Flash	PRAM	MRAM	FeRAM	NRAM
Read speed	Fastest	Medium	Fast	Fast	Fast	Fast	Fast
Write speed	Fastest	Medium	Slow	Fast	Fast	Med.	Fast
Cell density	Low	High	Medium	High	High	Med.	High
Process technology, nm	130	80	56	90	130	130	22
Nonvolatility	No	No	Yes	Yes	Yes	Yes	Yes
Future scalability	Good	Limited	Limited	Exell.	Good	Limited	Scalable

Magnetoresistive random-access memory

Phase-change memory

Ferroelectric RAM

Nano-RAM

Flash Memory