MMIC Design and Technology

Fabrication of MMIC

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Process Choice

- Substrate
  - Mobility & Peak Velocity: Frequency Response
  - Band-Gap Energy: Breakdown Voltage (Power-Handling)
  - Resistivity: Loss and Q of the Passives
- Transistor
  - Field-Effect Transistors
  - Bipolar Transistors

Most Commonly Used Semiconductors

Material	Electron Mobility (cm^2 /Vs)	Peak Velocity (10^7 cm/s)	Frequency Range (GHz)	Noise Figure	Gain	Maturity
Si	900 – 1,100	0.3 – 0.7	< 20	Moderate	Moderate	Mature 12-in Wafer
SiGe	2,000 – 300,000	0.1 – 1.0	10 – 40	Lower	Better	Mature 6-in Wafer
SiC	500 – 1,000	0.15 – 0.2	15 – 20	Poor	Lower	4-in Wafer
GaAs	5,500 – 7,000	1.6 – 2.3	➢75	Lower (F_{min} = 1.1)	Higher (G_{ass} = 9)	3, 4, 6-in Wafers
GaN	400 – 1,600	1.2 – 2.0	20 – 30	Poor	Lower	2-in Wafer
InP	10,000 – 12,000	2.5 – 3.5	➢115	Lower (F_{min} = 0.9)	Higher (G_{ass} = 11)	2-in Wafer

Transistors

	CMOS	SiGe HBT	GaAs/InP HBT	MESFET	HEMT
Oscillator	–	√	√	–	–
Mixer	–	√	√	–	–
LNA	–	√	√	–	√
Power Amplifier	–	–	√	–	√
Switch	–	–	–	√	√
Digital	√	√	–	–	–

MMIC

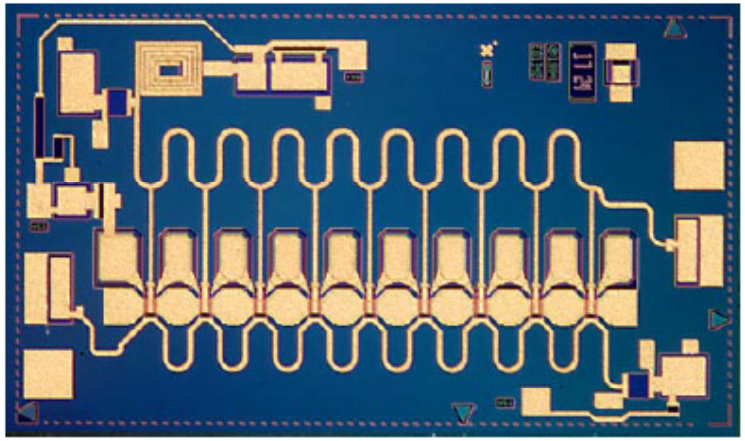
TriQuint SEMICONDUCTOR

Product Data Sheet

2-20 GHz Wideband AGC Amplifier

TGA1342-SCC

May 28, 2004



Chip Dimensions: 3.4 x 2.0 x 0.1 mm

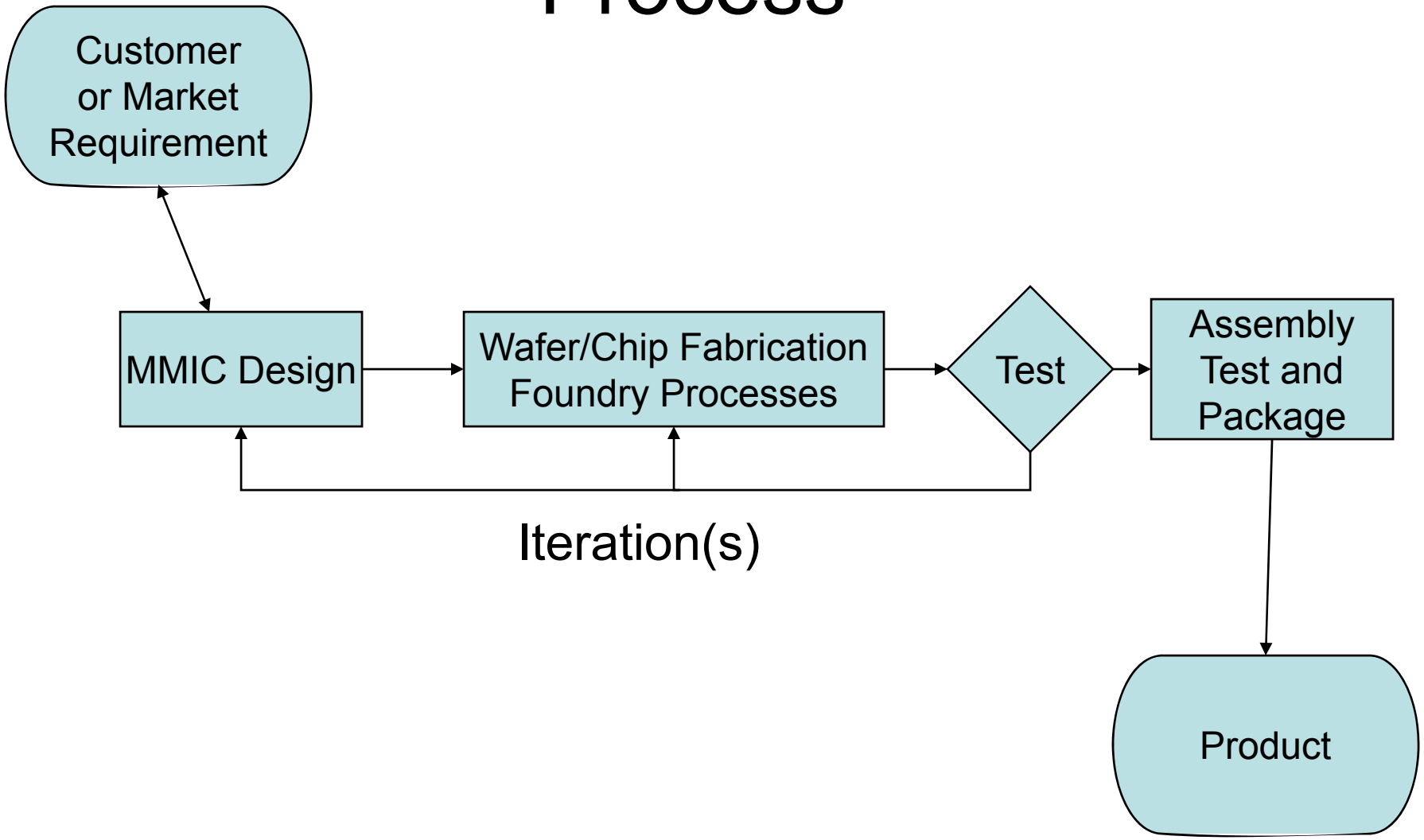
Key Features and Performance

- 0.5 um MESFET Technology
- 9 dB Nominal Gain
- 3.5 dB NF Typical Midband
- 17.5 dBm Nominal Pout @ P1dB
- Bias 5-8V @ 60 mA
- Dimensions 3.4 x 2.0 x 0.1 mm

Primary Applications

- Wideband Gain Block / LN Amplifier
- X-Ku Point to Point Radio
- IF & LO Buffer Applications

MMIC Product Develpoment Process



Why GaAs

- High Electron Mobility
  - High frequency operation
- Intrinsic GaAs is Semi-Insulating
  - Well suited for use as a substrate for stripline and passives
  - High Q
- Large Band Gap 1.4eV
  - High voltage = higher power
  - Radiation hard

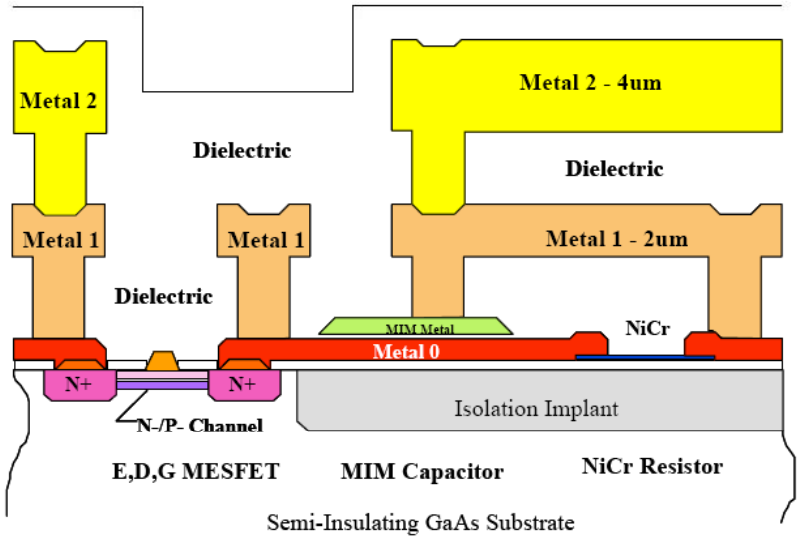
MMIC Production Process

Production Process

TriQuint SEMICONDUCTOR

TQTRx

GaAs MESFET Foundry Service



TQTRx Process Cross-Section

Features

- 0.6 µm Gate Length MESFET Process
- 4 Active Devices:
  - Power & Gain D-FETs
  - E-FET
  - Schottky-Barrier Diodes
- High Density Interconnects:
  - 2 Global and 1 local
  - 6 µm total thickness
- High-Q Passives
- Bulk & Thin Film Resistors
- High Value Capacitors
- Dielectric Encapsulated Metals
- Planarized Surface; simplified plastic packaging
- Substrate Vias Available
- Volume Production Process
- Validated Models and Design Support

FET

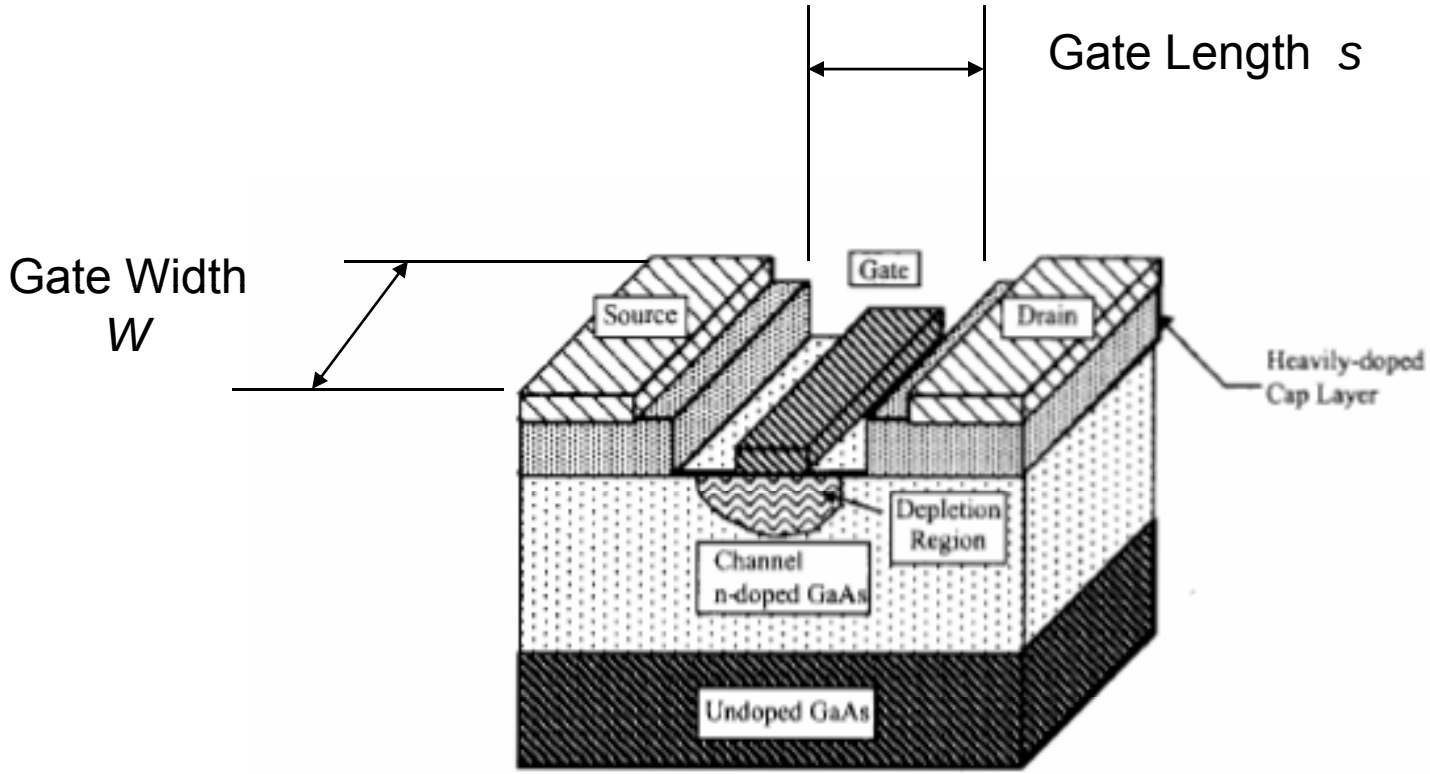
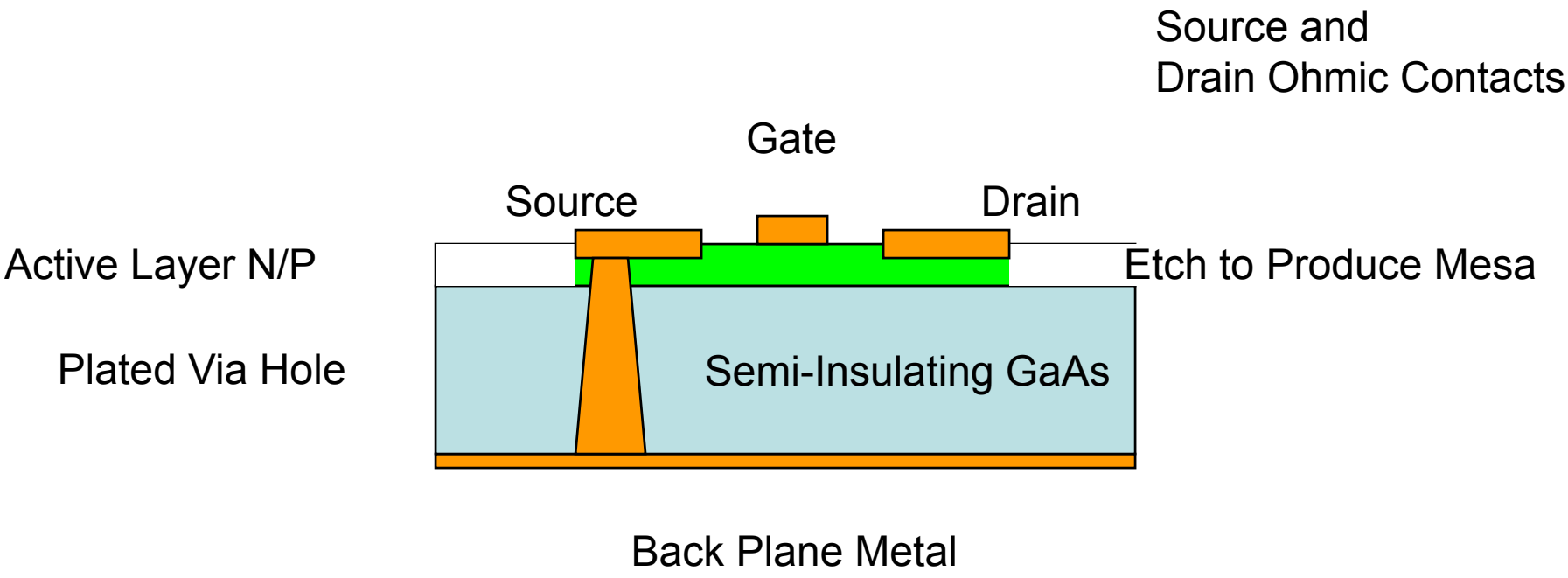


Figure 2.27 Cross-section of a MESFET device

MESFET


Source and
Drain Ohmic Contacts
Gate
Source
Drain
Active Layer N/P
Etch to Produce Mesa
Plated Via Hole
Semi-Insulating GaAs
Back Plane Metal

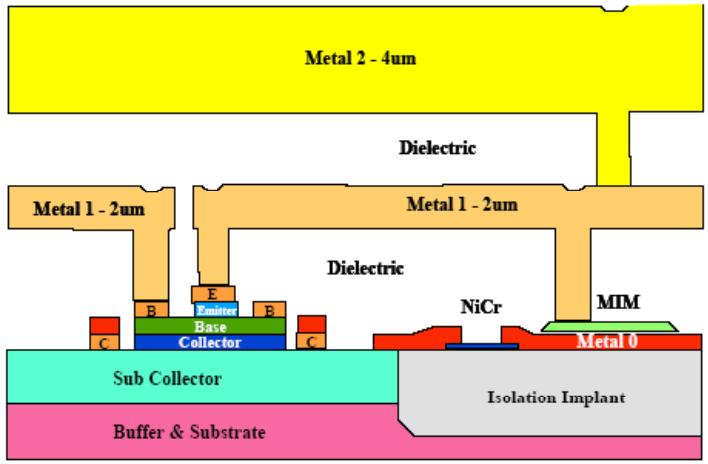
HBT Process

Production Process

TriQuint SEMICONDUCTOR

TQHBT3

InGaP HBT Foundry Service

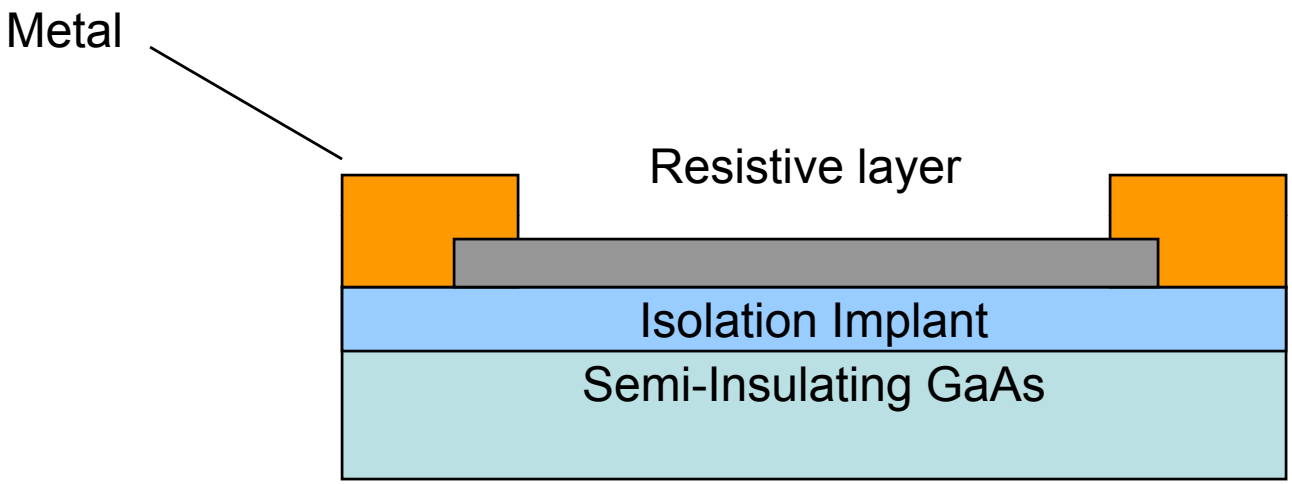


TQHBT3 Process Cross-Section

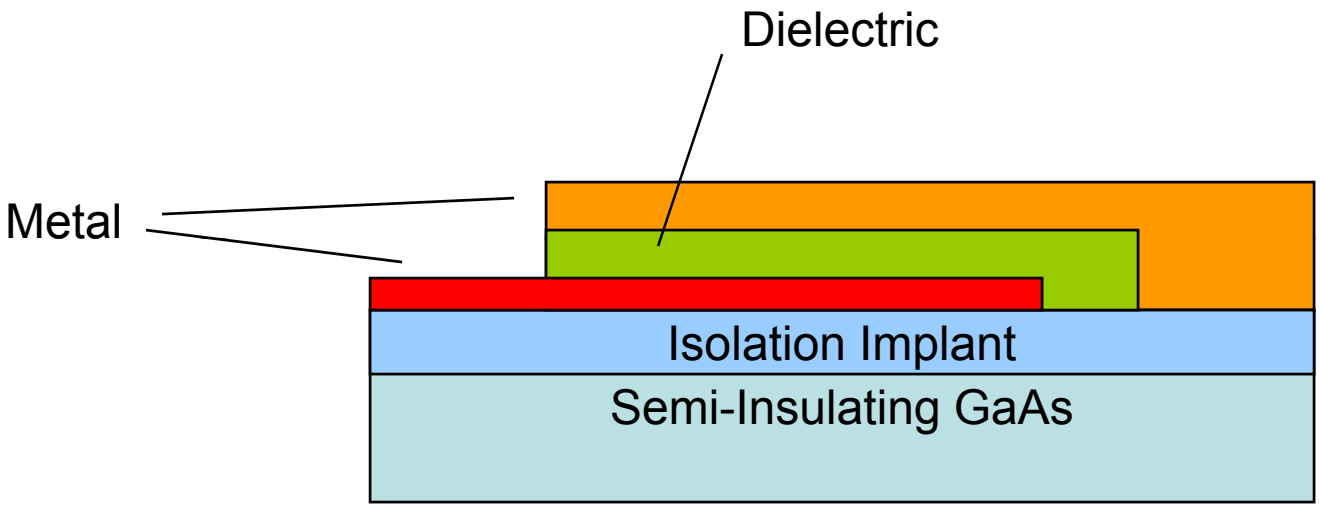
Features

- 2– and 3-um emitter widths
- >22 dB MAG @ 6 GHz; with 3-um emitters
- Amplifier Ruggedness: VSWR 70:1 @ 5 V supply
- High Linearity in PA applications
- InGaP Emitter Process for High Reliability and Thermal Stability
- Base Etch Stop for Uniformity
- MOCVD Epitaxy
- High Density Interconnects;
  - 2 Global, 1 Local
  - Over 6 µm Total Thickness
  - Dielectric Encapsulated Metals
- Thick Metal Interconnects:
  - Enhanced Thermal Management
  - Minimum Die Size

Resistor


Metal
Resistive layer
Isolation Implant
Semi-Insulating GaAs

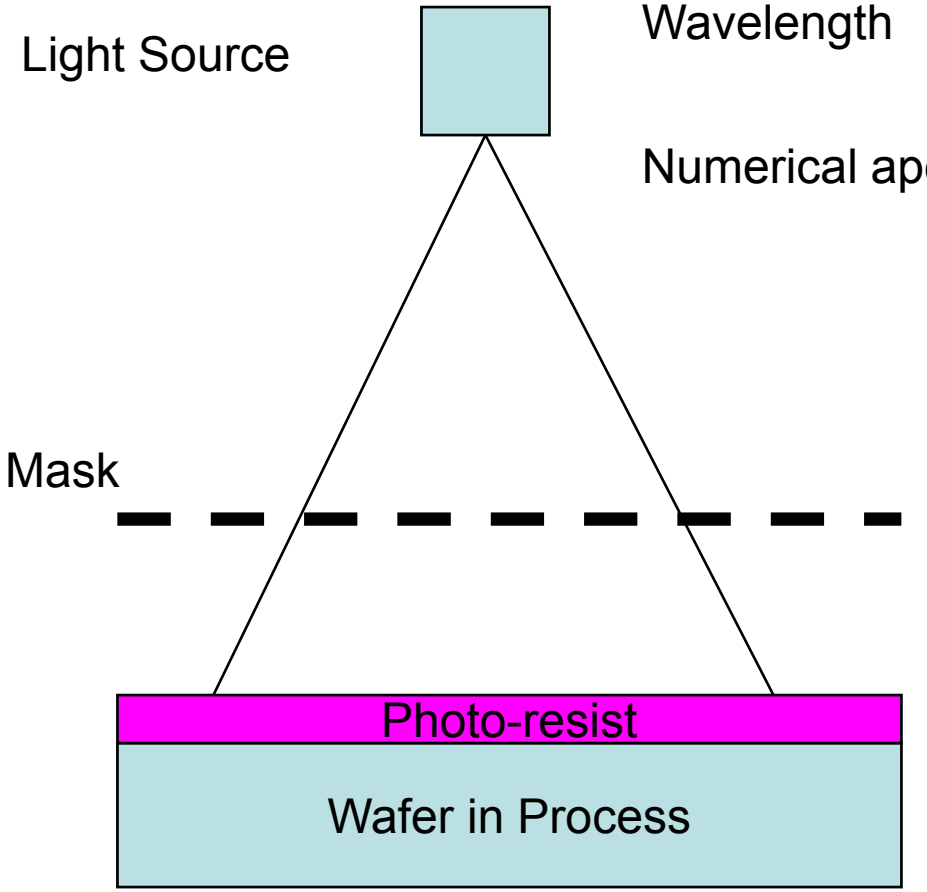
Capacitors



Process list

Wafer fabrication
Wet cleans
Photolithography
Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
Dry Etching
Wet Etching
Plasma ashing
Thermal treatments
Rapid thermal anneal
Furnace anneals
Oxidation
Chemical vapor deposition (CVD)
Physical vapor deposition(PVD)
Molecular beam epitaxy (MBE)
Electroplating
Chemical mechanical polish (CMP)
Wafer testing (where the electrical performance is verified)
afer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card
Die preparation
Wafer mounting
Die cutting

Lithography



Wavelength λ

Numerical aperture NA

Resolution ***s***

$$s = \frac{k\lambda}{NA}$$

k Is a constant of the process

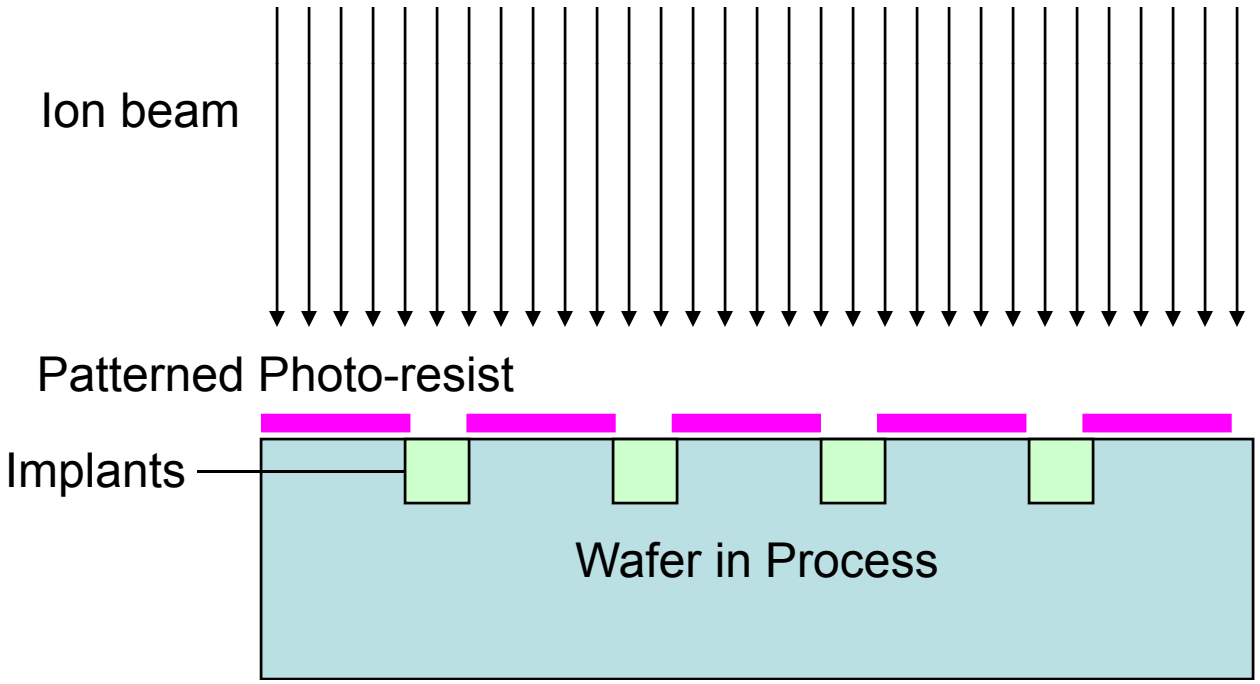
Lithography

- Optical
- UV
- Deep UV, X-UV
- Electron Beam
  - Voltage U
- Direct write e-beam
  - Electronically scanned
  - No mask

$$\lambda = \frac{h}{\sqrt{2m_0 eU}} \frac{1}{\sqrt{1+\frac{eU}{2m_0 c^2}}}$$

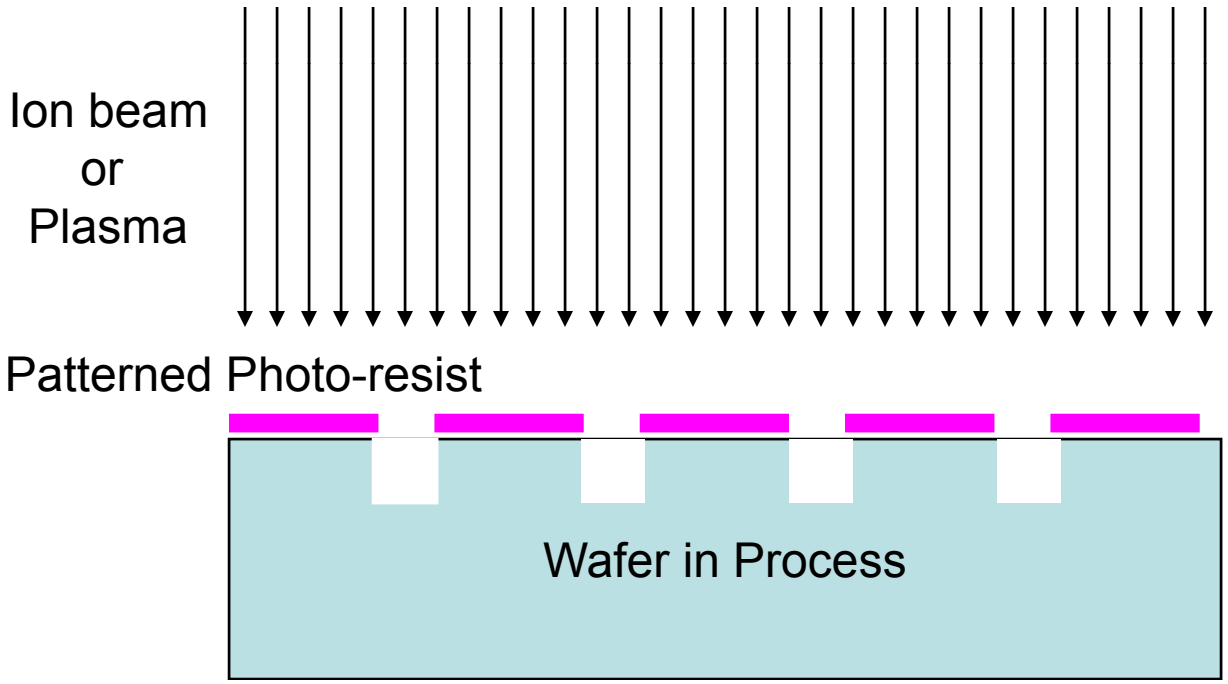
Ion Implantation

Selectively implant impurities
Create n or p type semiconductor regions



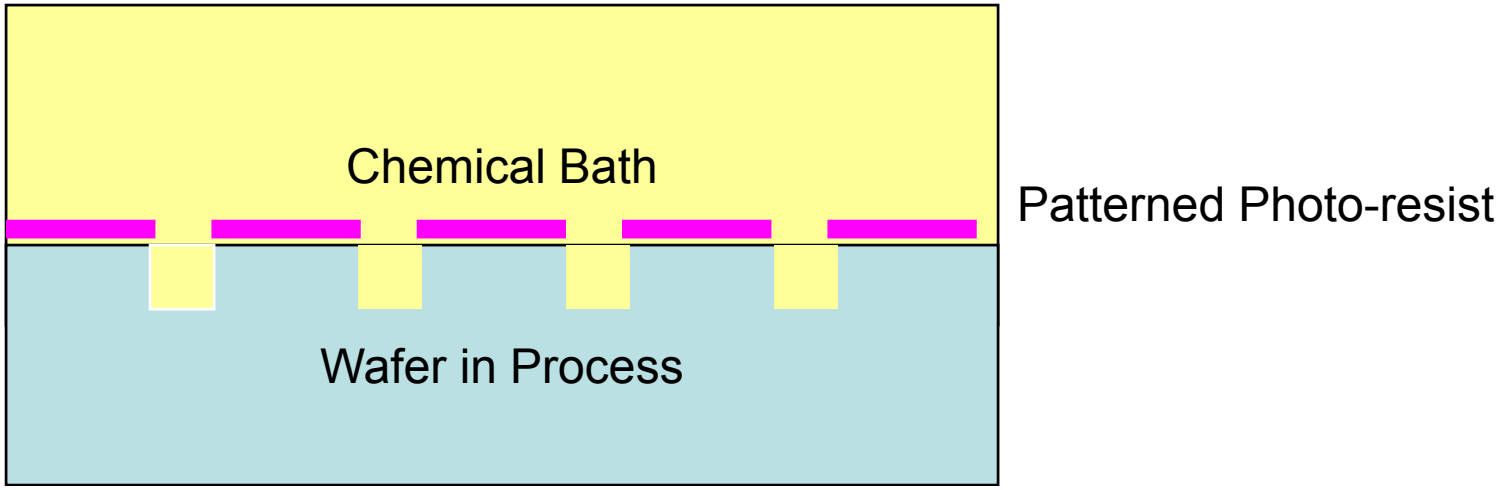
Ion etch

Selectively remove material
Dry Etch Process



Wet Etch

Selectively remove material
Chemical Process



MBE

- Molecular Beam Epitaxy
  - Selectively grow layers of material
- A beam of atoms or molecules produced in high vacuum
  - Deposited on wafer in a pattern defined by photoresist

CVD

- Chemical Vapor Deposition
  - A chemically produced vapor is deposited on the wafer
  - Pattern is defined by photoresist

PVD

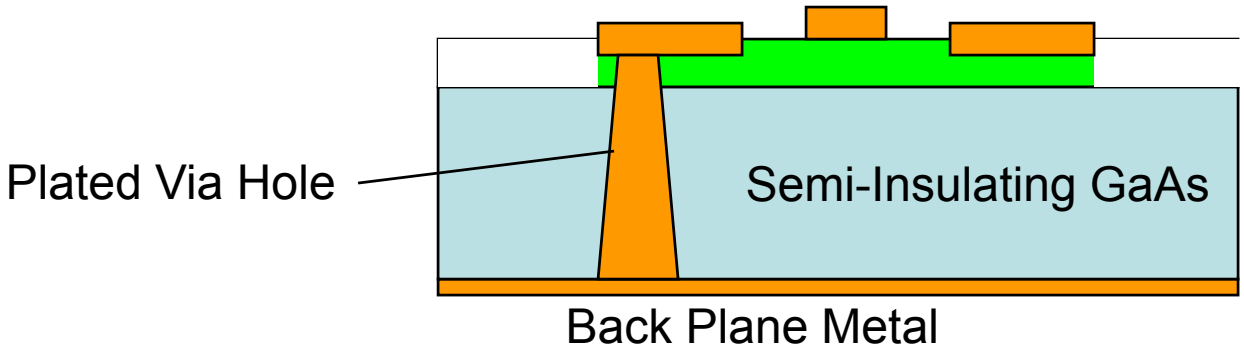
- Physical Vapor Deposition
  - A vapor is produced by evaporation or sputtering
  - Deposited on wafer
  - Pattern defined by Photoresist

Electroplate

- Electroplating is an electrochemical process used to add metal
- Plating used to increase thickness of metal layers

Backside Processing

- Via Holes
- Back Plane Metal



Thermal Annealing

- High temperature processing to remove stress between process steps

Example

Apply Resist

Expose Resist

Remove Resist

Isolation Implant Channel Dope Contact Dope

Remove Resist