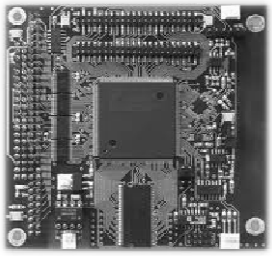
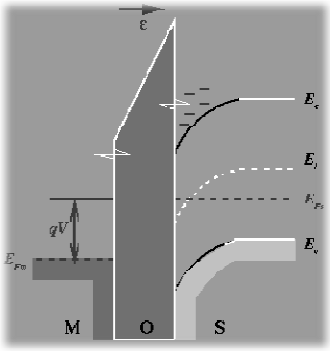


Session 6: MOSFET

Solid State Devices:

1



MOSFET: 2Terminal

MOS Capacitance

2

MS Junctions - Before being joined

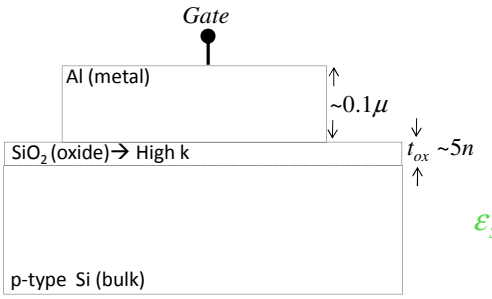
Metal: Al, …, Poly Si (n^{++},p^{++}), $\rho_{poly}=0.1^{m\Omega\text{-cm}}$

Oxide: SiO_2 (reason why Si beat GaAs)

Semi Conductor: Si

CMOS is the dominant technology in integrated circuits

Heart of a MOSFET is MOS-cap



p-type bulk → nMOS

n-type bulk → pMOS

(n/p)MOS → CMOS

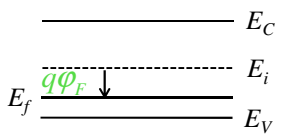
$$\varepsilon_{Si}=11.9,(\sim 3\times)\varepsilon_{SiO_2}=3.9$$

3

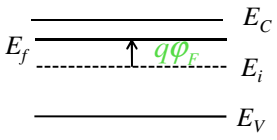
Bulk Semiconductor Potential, ϕ_F

Definition:

$$q\varphi_F \triangleq E_i - E_F = E_{i(bulk)} - E_F$$



p-type



n-type

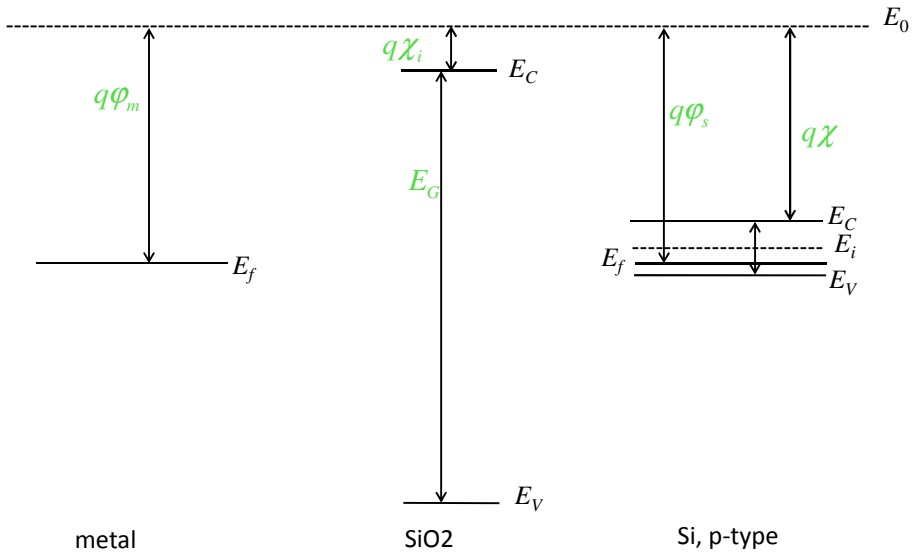
$$q\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) > 0$$

$$q\varphi_F = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) < 0$$

4

M O S – Special case

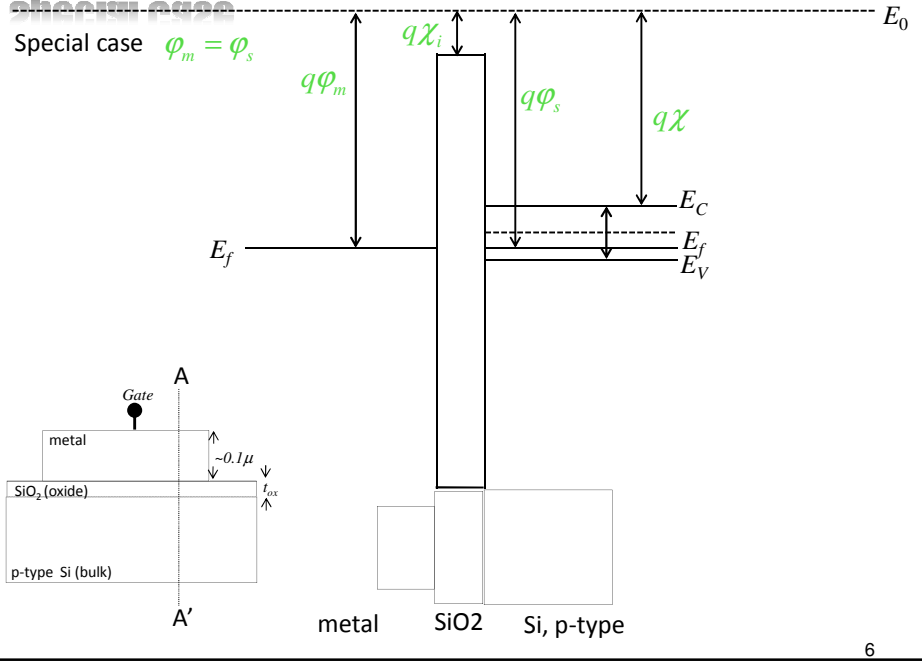
Special case $\varphi_m = \varphi_s$



5

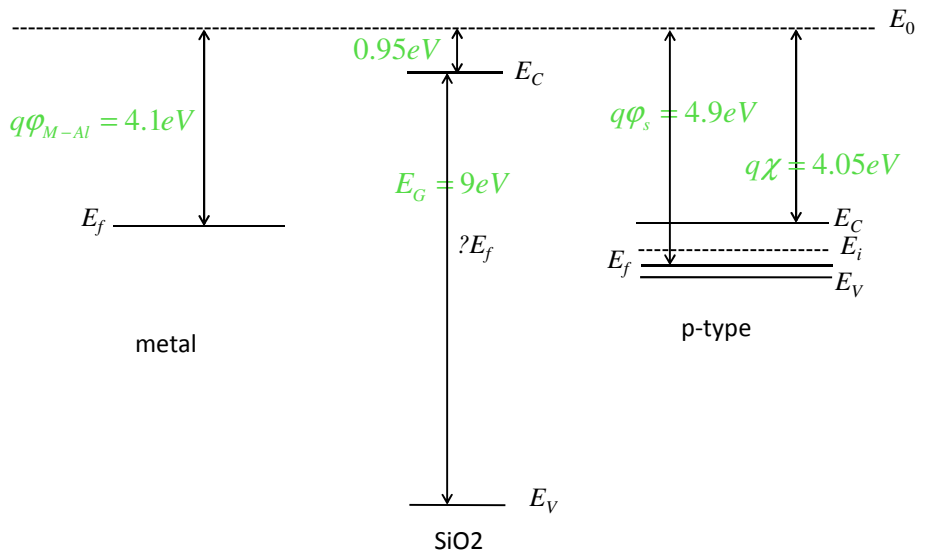
Special Case

Special case $\varphi_m = \varphi_s$



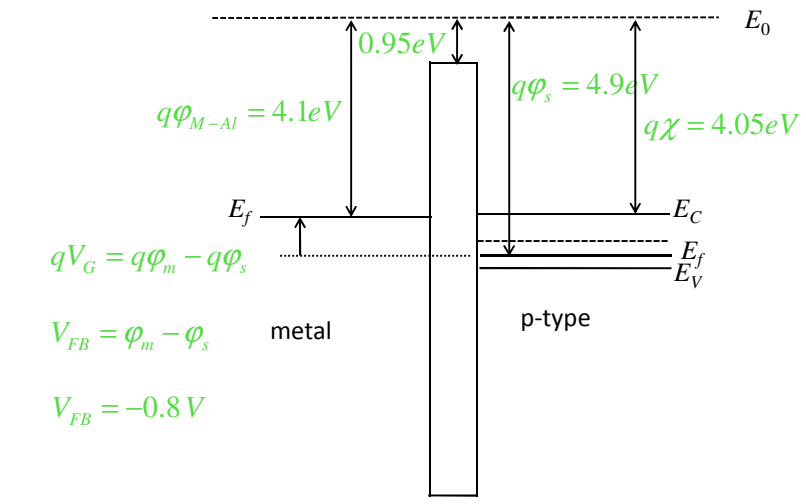
6

M (Al) O (SiO2) S (Si)



7

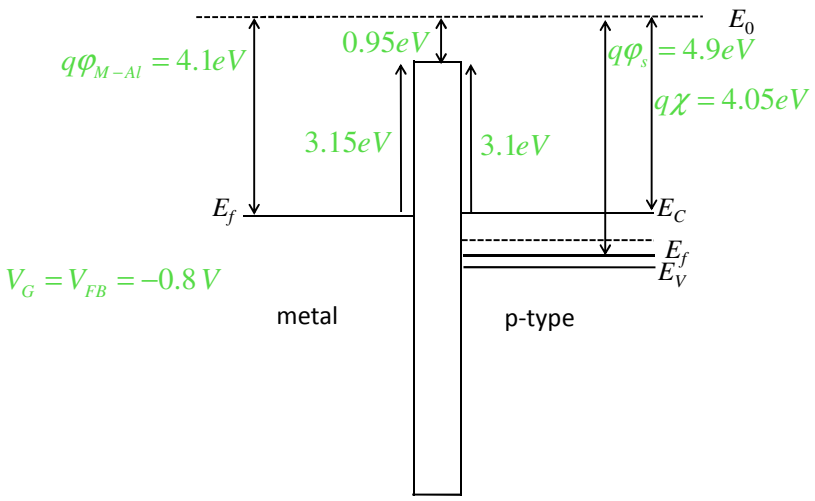
Flat Band Voltage



8

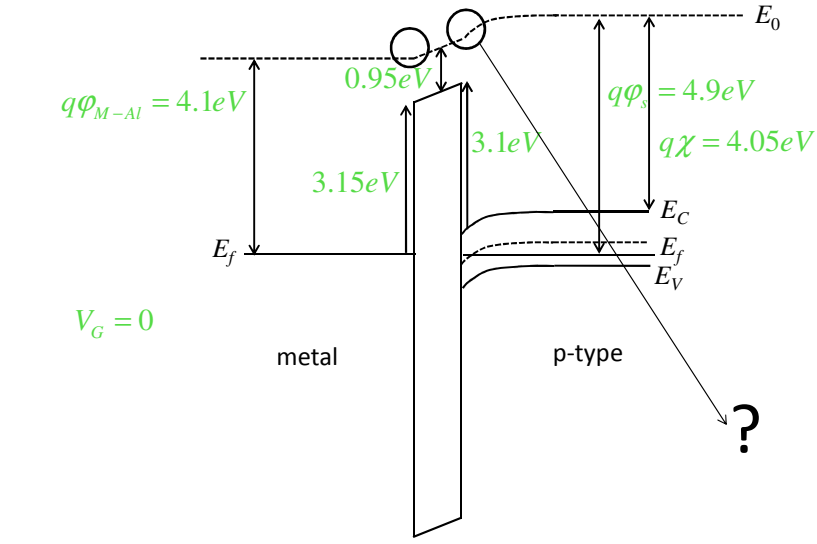
Voltage barrier

No way electrons might pass the voltage barrier!



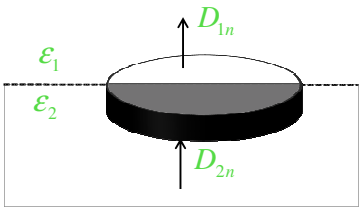
9

No Gate voltage



10

Boundary conditions



$$D_{2n} - D_{1n} = \rho_{surface}$$

$$\rho_{surface} = 0$$

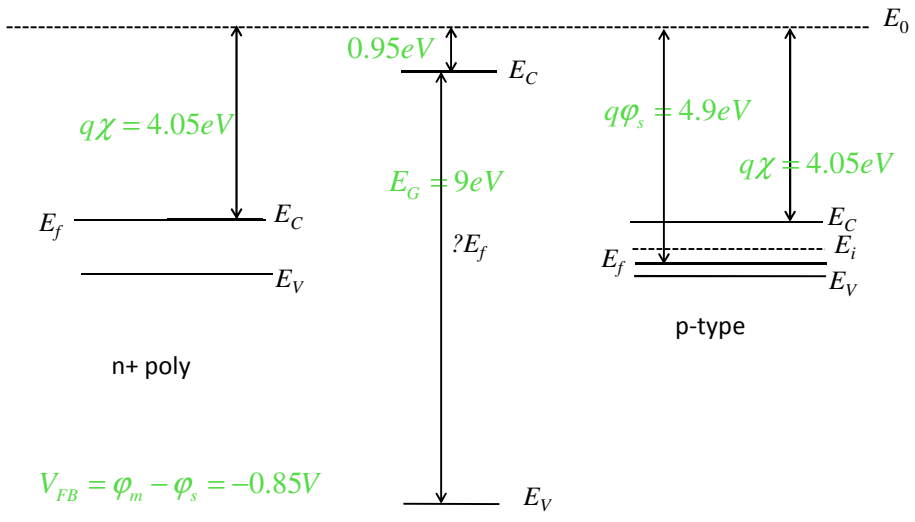
$$\varepsilon_1 \mathcal{E}_{1n} = \varepsilon_2 \mathcal{E}_{2n}$$

$$\varepsilon_{SiO_2} \left.\frac{dE_{ox}}{dx}\right|_{\text{int}} = \varepsilon_{Si} \left.\frac{dE_{Si}}{dx}\right|_{\text{int}}$$

$$\left.\frac{dE_{ox}}{dx}\right|_{\text{int}} \approx 3 \left.\frac{dE_{Si}}{dx}\right|_{\text{int}}$$

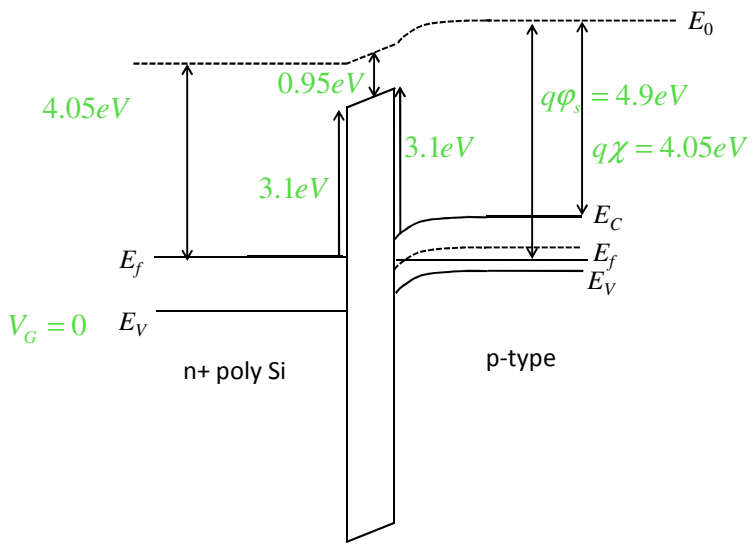
11

Poly Gate



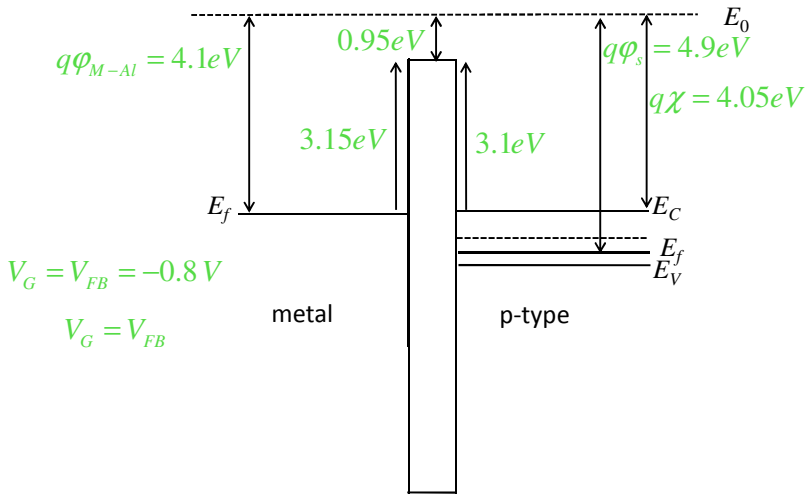
12

Poly Gate



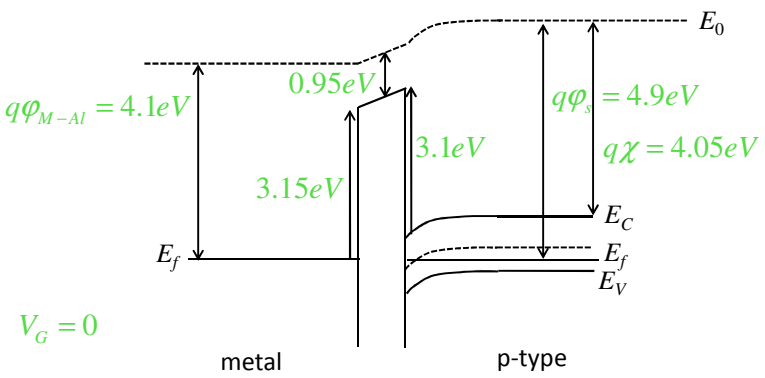
13

Flat Band



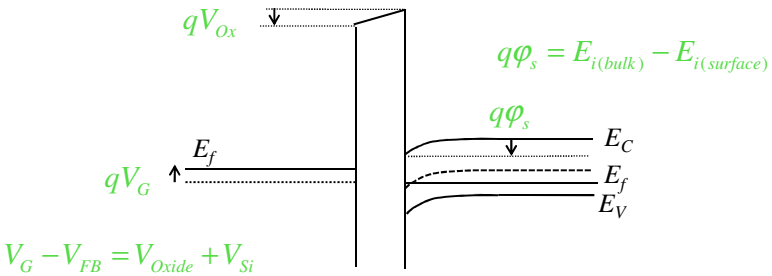
14

No Gate voltage



15

Gate voltage



$$V_G - V_{FB} = V_{Oxide} + V_{Si}$$
$$= V_{Ox} + \varphi_s$$

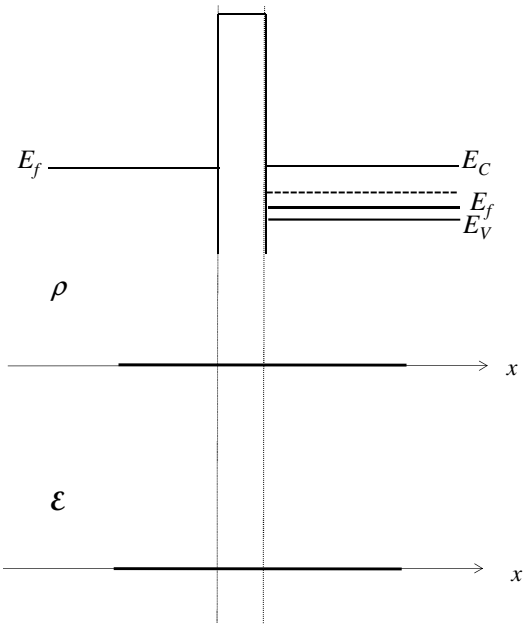
$$\boxed{V_G - V_{FB} = V_{Ox} + \varphi_s}$$

As important as KVL

16

Flat Band

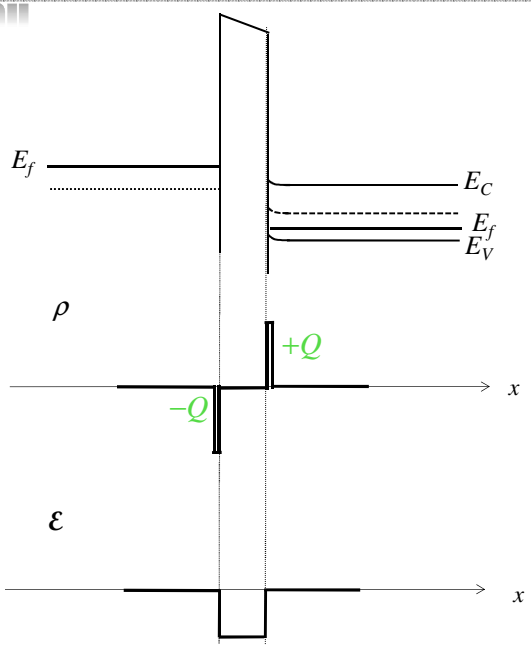
$V_G = V_{FB}$



17

Accumulation

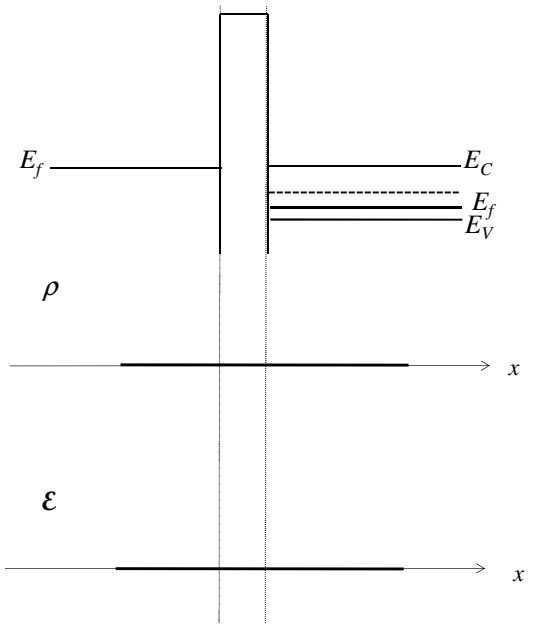
$V_G < V_{FB}$



18

Flat Band

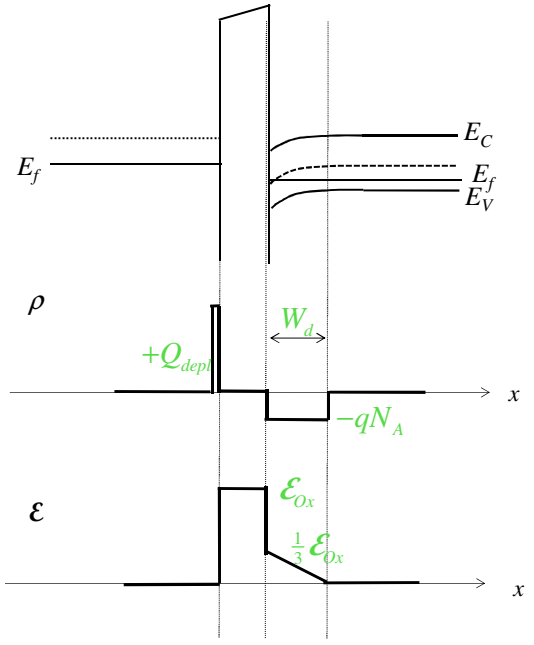
$V_G = V_{FB}$



19

Depletion

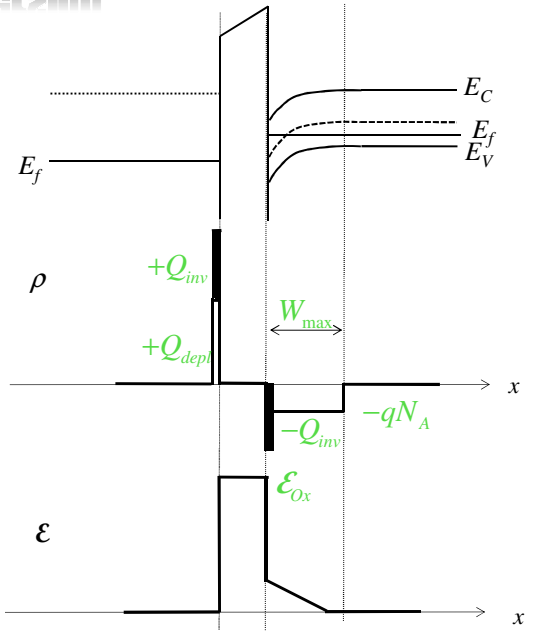
$V_T > V_G > V_{FB}$



20

(Strong) Inversion

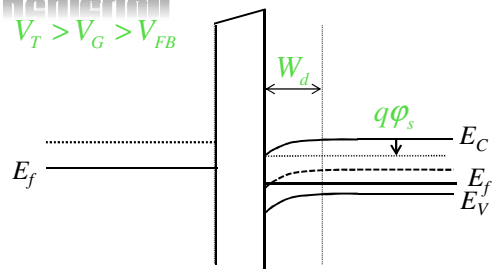
$V_G > V_T$



21

Depletion

$V_T > V_G > V_{FB}$



$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\varepsilon_{Si}} = \frac{-qN_A}{\varepsilon_{Si}} = \frac{d^2\varphi}{dx^2} \rightarrow$$

$$\varphi_s = \frac{qN_A x^2}{2\varepsilon_{Si}} \rightarrow W_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}\varphi_s}$$

$$\mathcal{E}_{ox} = \frac{-Q_{dep}}{\varepsilon_{ox}} \rightarrow V_{ox} = \frac{-Q_{dep}t_{ox}}{\varepsilon_{ox}} = \frac{-Q_{dep}[C/cm^2]}{C_{ox}[F/cm^2]}$$

$$Q_{dep} = -qN_A W = -\sqrt{2qN_A\varepsilon_{Si}\varphi_s}$$

$$V_G = V_{FB} + V_{ox} + \varphi_s \rightarrow V_G = V_{FB} + \varphi_s + \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}\varphi_s}$$

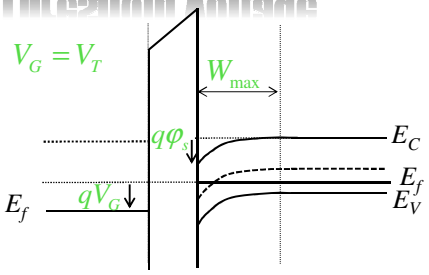
p-type Si (nMOS) In Depl

$$\varphi_s < 0 \qquad V_G = V_{FB} + \varphi_s - \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}|\varphi_s|}$$

n-type Si (pMOS) In Depl

22

Threshold Voltage



$$V_T = V_G\big|_{\varphi_s = 2\varphi_F}$$

$$n_{surface} = N_A \qquad p_{bulk} = N_A$$

$$W_{max} = W_T\big|_{\varphi_s = 2\varphi_F} = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}(2\varphi_F)}$$

Definition of Threshold voltage:

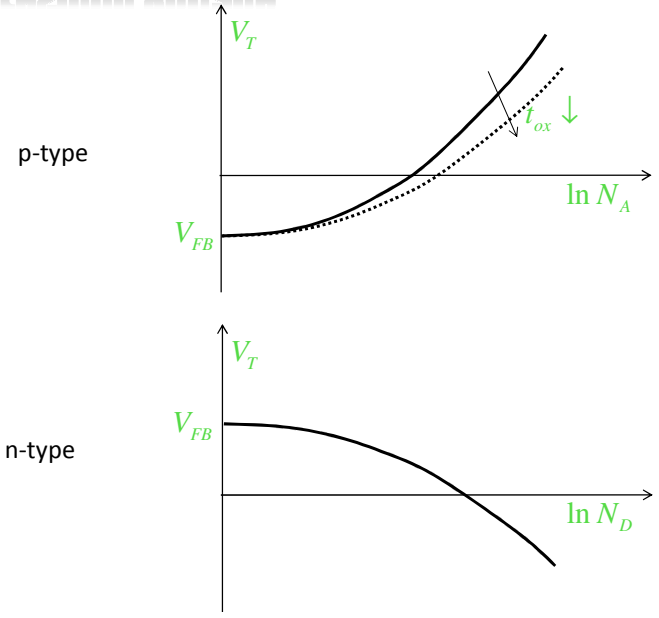
p-type $$V_T = V_G\big|_{\varphi_s = 2\varphi_F} = V_{FB} + 2\varphi_F + \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}(2\varphi_F)}$$

$$\left(\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right)$$

n-type $$V_T = V_{FB} + 2\varphi_F + \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}|2\varphi_F|} \qquad \left(\varphi_F = -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)\right)$$

23

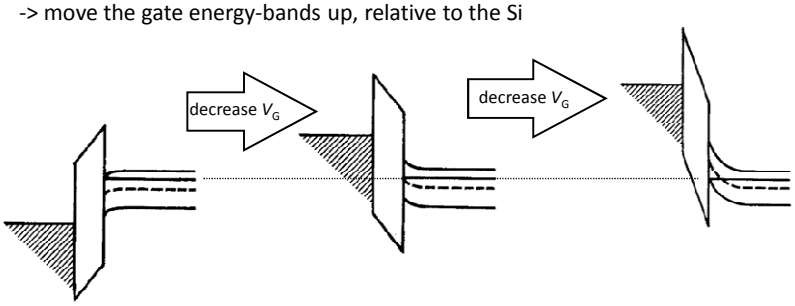
Threshold Voltage



24

MOS Band Diagrams (n-type Si)

Decrease V_G (toward more negative values)
-> move the gate energy-bands up, relative to the Si

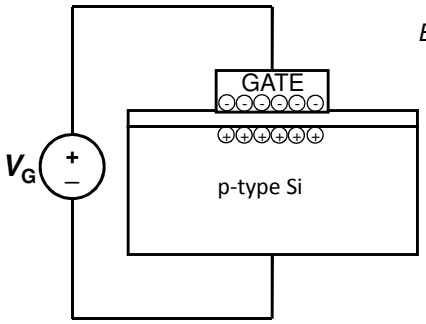


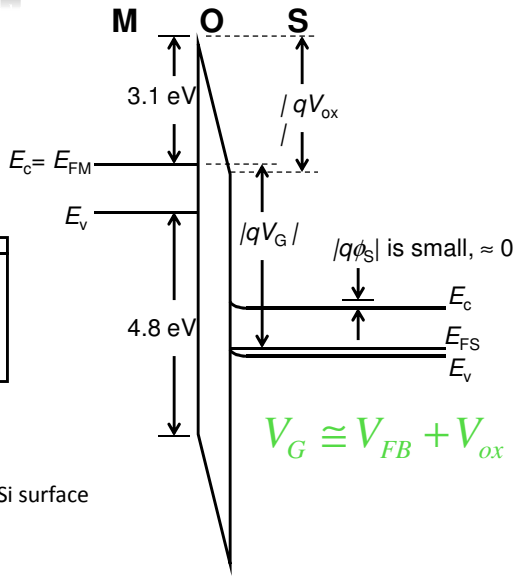
- Accumulation
  - $V_G > V_{FB}$
  - Electrons accumulate at surface
- Depletion
  - $V_G < V_{FB}$
  - Electrons repelled from surface
- ⊙ Inversion
  - $V_G < V_T$
  - Surface becomes p-type

25

Accumulation, Poly gate

$V_G < V_{FB}$





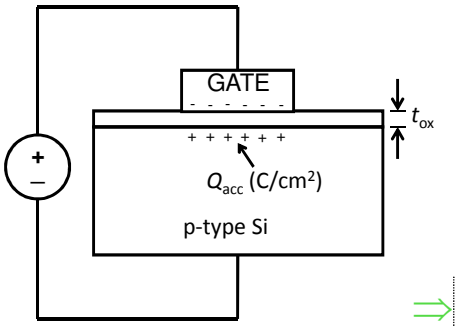
$$V_G \cong V_{FB} + V_{ox}$$

Mobile carriers (holes) accumulate at Si surface

26

Accumulation Layer charge density

$V_G < V_{FB}$



$$V_{ox} \cong V_G - V_{FB}$$

From Gauss' Law:

$$\mathcal{E}_{ox} = -Q_{acc} / \varepsilon_{SiO_2}$$

$$V_{ox} = \mathcal{E}_{ox} t_{ox} = -Q_{acc} / C_{ox}$$

where $C_{ox} \equiv \varepsilon_{SiO_2} / t_{ox}$

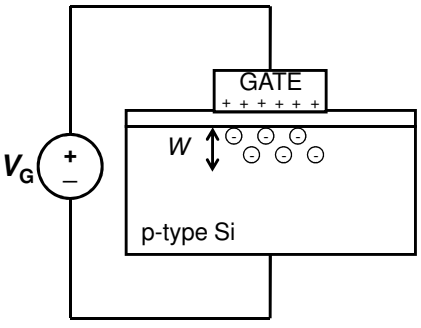
(units: F/cm²)

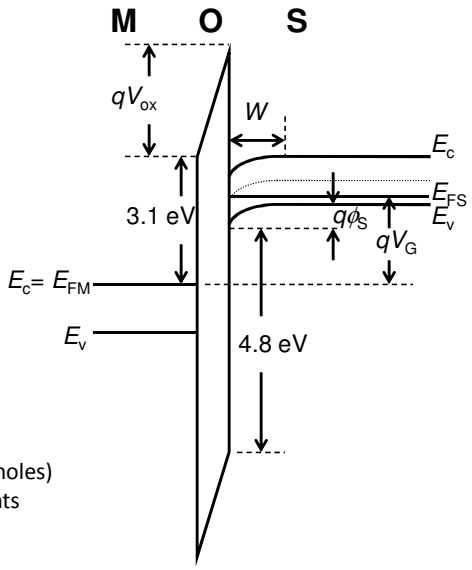
$$\Rightarrow \boxed{Q_{acc} = -C_{ox}(V_G - V_{FB}) > 0}$$

27

Depletion (n+ poly-Si gate, p-type Si)

$V_T > V_G > V_{FB}$



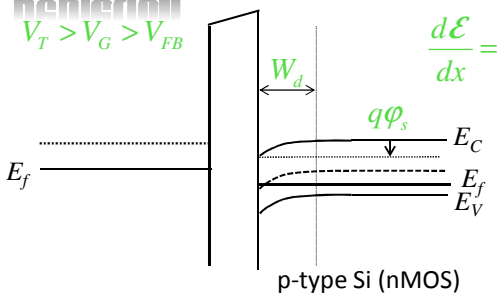


Si surface is depleted of mobile carriers (holes)
=> Surface charge is due to ionized dopants (acceptors)

28

Depletion

$V_T > V_G > V_{FB}$



p-type Si (nMOS)

$$\frac{d\mathcal{E}}{dx} = \frac{-qN_A}{\varepsilon_{Si}} = \frac{d^2\varphi}{dx^2} \rightarrow \varphi_s = \frac{qN_A x^2}{2\varepsilon_{Si}}$$

$$\rightarrow W_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}\varphi_s}$$

$$V_{ox} = \frac{-Q_{dep}}{C_{ox}}$$

$$V_G = V_{FB} + V_{ox} + \varphi_s \rightarrow V_G = V_{FB} + \varphi_s + \frac{1}{C_{ox}}\sqrt{2qN_A\varepsilon_{Si}\varphi_s}$$

Solving for ϕ_S

$$\varphi_S = \frac{qN_A\varepsilon_{si}}{2C_{ox}^2}\left[\sqrt{1+\frac{2C_{ox}^2(V_G - V_{FB})}{qN_A\varepsilon_{si}}} - 1\right]^2$$

$$Q_{dep} = -qN_A W = -\sqrt{2qN_A\varepsilon_{Si}\varphi_s}$$

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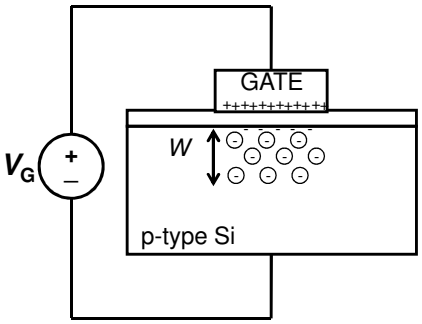
Strong Inversion (p-type Si)

As V_G is increased above V_T, the negative charge in the Si is increased by adding mobile electrons (rather than by depleting the Si more deeply), so **the depletion width remains ~constant at $W = W_T$**



Significant density of mobile electrons at surface (surface is n-type)

$$\varphi_S \cong 2\varphi_F \rightarrow W \cong W_T = \sqrt{\frac{2\varepsilon_{si}(2\varphi_F)}{qN_A}}$$

$$V_G = V_{FB} + \varphi_S + V_{ox}$$

$$= V_{FB} + 2\varphi_F - \frac{(Q_{dep} + Q_{inv})}{C_{ox}}$$

$$= V_{FB} + 2\varphi_F + \frac{\sqrt{2qN_A\varepsilon_s(2\varphi_F)}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

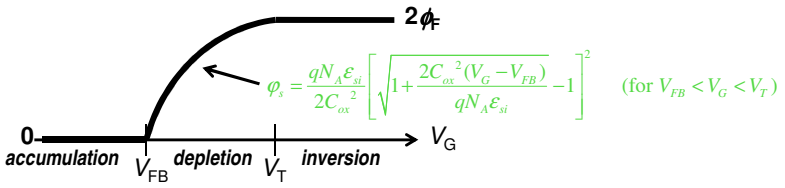
$$= V_T - \frac{Q_{inv}}{C_{ox}}$$

$$\therefore \quad Q_{inv} = -C_{ox}(V_G - V_T)$$

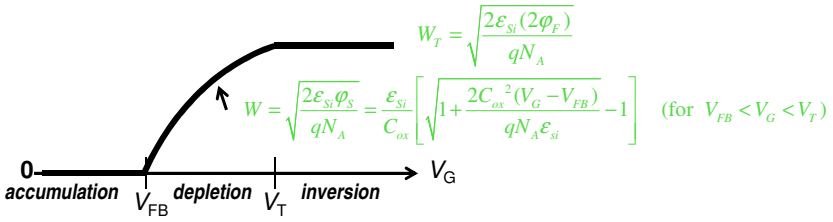
30

ϕ_s and W vs. V_G (p-type Si)

ϕ_S:

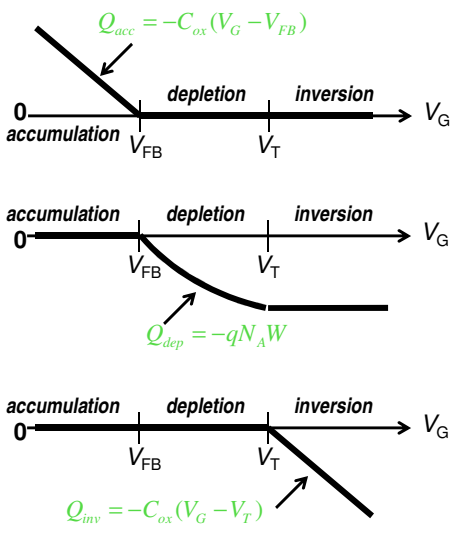


W:

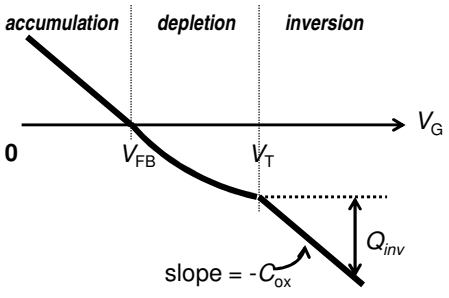


31

Total Charge Density in Si, Qs



$$Q_s = Q_{acc} + Q_{dep} + Q_{inv}$$



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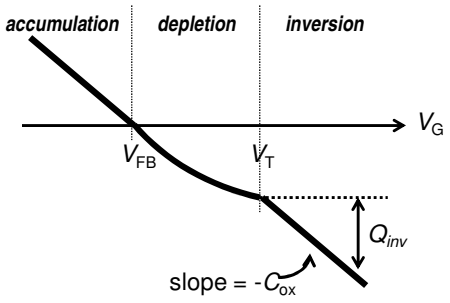
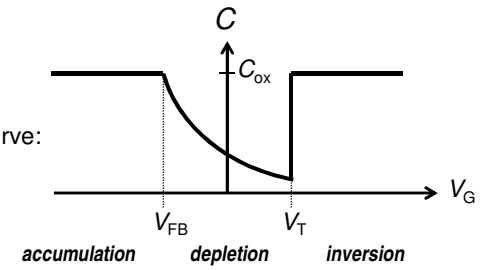
MOS C-V Characteristics (p-type Si)



$$C = \left|\frac{dQ_{GATE}}{dV_G}\right| = \left|\frac{dQ_s}{dV_G}\right|$$

Ideal *C-V* curve:



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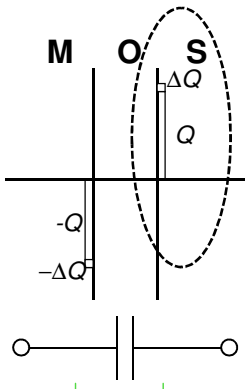
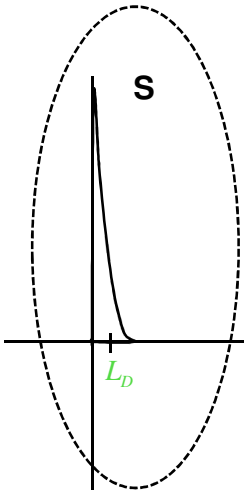
Debye Length

- As the gate voltage is varied, incremental charge is added/subtracted to/from the gate and substrate.
- The incremental charges are separated by the gate oxide.



$$C = \left|\frac{dQ_{acc}}{dV_G}\right| = C_{ox}$$



$$\frac{d^2\varphi}{dx^2} = -\frac{\rho}{\varepsilon} =$$

$$\frac{q}{\varepsilon}(N_D - N_A + p - n)$$

For n-type bulk:

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon}(N_D - n)$$

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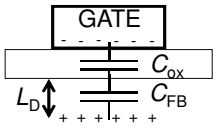
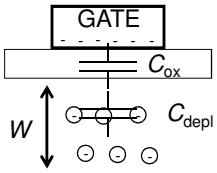
Flat-Band Capacitance

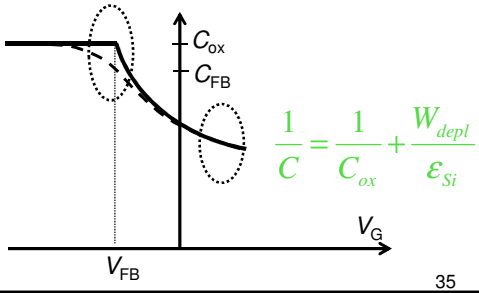
$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon}(N_D - n) = \frac{q}{\varepsilon}(N_D - n_i e^{q(\varphi_n - \varphi)/kT}) = \frac{q}{\varepsilon} N_D (1 - e^{q\varphi/kT})$$

Taylor series: $\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon} N_D \frac{q\varphi}{kT} = \frac{\varphi}{L_D^2}$ $\left(L_D = \sqrt{\frac{\varepsilon kT}{q^2 N_D}} \right)$



$$C_{FB} = \frac{C_{ox} C_D}{C_{ox} + C_D} \rightarrow \frac{1}{C_{FB}} = \frac{t_{ox}}{\varepsilon_{ox}} + \frac{L_D}{\varepsilon_{Si}}$$





$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{W_{depl}}{\varepsilon_{Si}}$$

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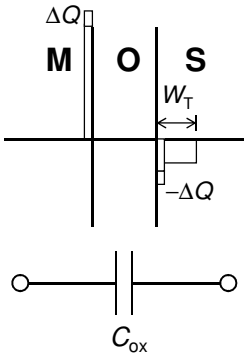
Capacitance in Inversion (p-type Si)

CASE 1: Inversion-layer charge *can* be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at the surface of the substrate.



Time required to build inversion-layer charge = $2N_A\tau_o/n_i$, where
τ_o = minority-carrier lifetime at surface

$$C = \left| \frac{dQ_{inv}}{dV_G} \right| = C_{ox}$$

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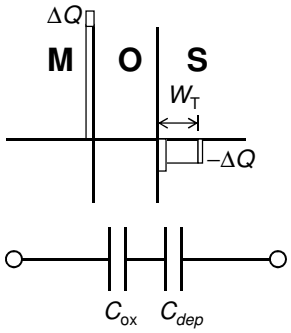
Capacitance in Inversion (p-type Si)

CASE 2: Inversion-layer charge *cannot* be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at a depth W_T in the substrate.



$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{ox}} + \frac{W_T}{\varepsilon_{Si}}$$

$$= \frac{1}{C_{ox}} + \sqrt{\frac{2(2\varphi_F)}{qN_A\varepsilon_{Si}}} \equiv \frac{1}{C_{\min}}$$

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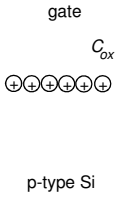
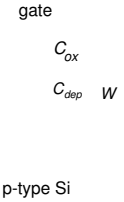
Supply of Substrate Charge (p-type Si)

Accumulation:

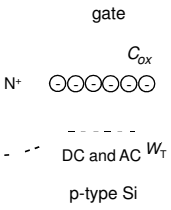


Depletion:

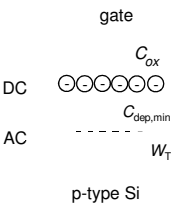


Inversion:

Case 1



Case 2



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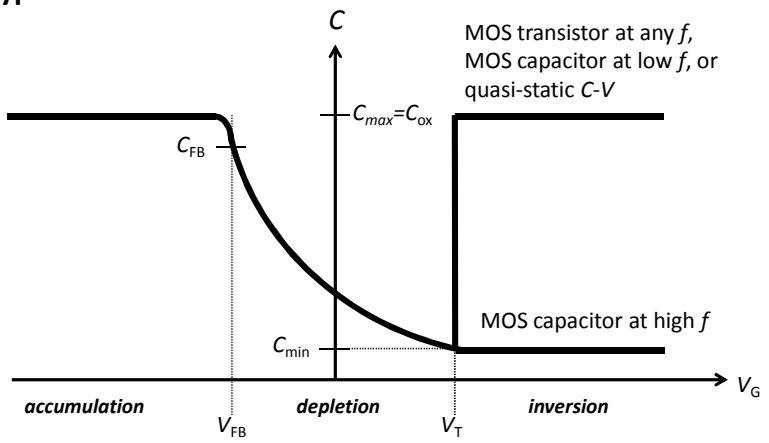
Capacitor vs. Transistor C-V (LF vs. HF)

p-type Si:



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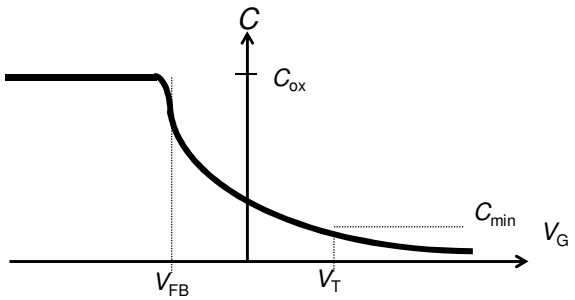
Deep Depletion

If V_G is scanned quickly, Q_{inv} cannot respond to the change in V_G. The increase in substrate charge density Q_s must then come from an increase in depletion charge density Q_{dep}

$\Rightarrow$ depletion depth W increases as V_G increases

$\Rightarrow$ C decreases as V_G increases



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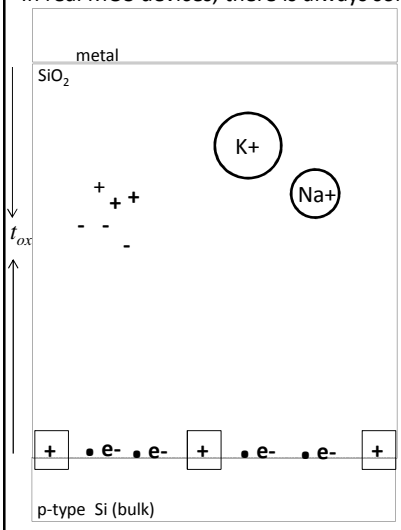
Oxide Charges

In real MOS devices, there is always some charge in the oxide and at the Si/oxide interface.



In the oxide:

1. Trapped charge Q_{ot}
   High-energy electrons and/or holes injected into oxide
2. Mobile charge Q_M
   Alkali-metal ions, which have sufficient mobility to drift in oxide under an applied electric field

At the interface:

1. Fixed charge Q_F
   Excess Si (+)
2. Trapped charge Q_{IT}
   Dangling bonds

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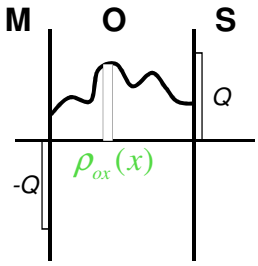
Effect of Oxide Charges



In general, charges in the oxide cause a shift in the gate voltage required to reach the threshold condition:

$$\Delta V_T = -\frac{1}{\varepsilon_{SiO_2}} \int_0^{x_o} x \rho_{ox}(x) dx$$

(x defined to be 0 at metal-oxide interface)

In addition, they may alter the field-effect mobility of mobile carriers (in a MOSFET) due to Coulombic scattering

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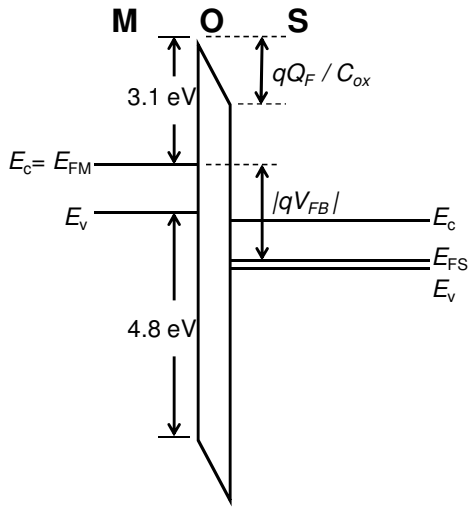
Fixed Oxide Charge Q_F



$$V_{FB} = \varphi_{MS} - \frac{Q_F}{C_{ox}}$$

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Parameter Extraction from C-V

From a single *C-V* measurement, we can extract much information about the MOS device.

- Suppose we know that the gate-electrode material is heavily doped n-type poly-Si (Φ_M=4.05eV), and that the gate dielectric is SiO_2 (ε_r=3.9):
  - From $C_{max} = C_{ox}$ we determine the oxide thickness x_o
  - From C_{min} and C_{ox} we determine substrate doping (by iteration)
  - From substrate doping and C_{ox} we calculate the flat-band capacitance C_{FB}
  - From the *C-V* curve, we can find
  - From Φ_M, Φ_S, C_{ox}, and V_{FB} we can determine Q_f

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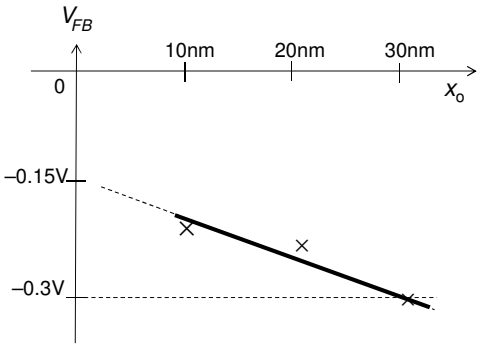
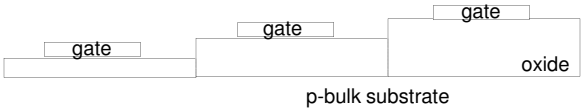
Determination of Φ_M and Q_F

Measure *C-V* characteristics of capacitors with different oxide thicknesses. Plot V_{FB} as a function of x_o:



$$V_{FB} = \varphi_{MS} - \frac{x_o}{\varepsilon_{SiO_2}} Q_F$$



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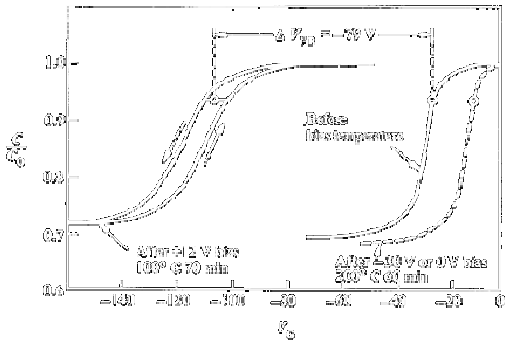
Mobile Ions

Odd shifts in *C-V* characteristics were once a mystery:



$$\Delta V_{FB} = -\frac{Q_M}{C_{ox}}$$

Source of problem: Mobile charge moving to/away from interface, changing charge centroid

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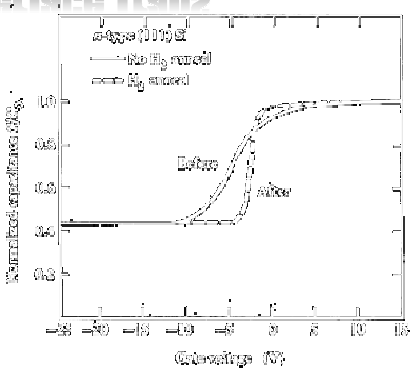
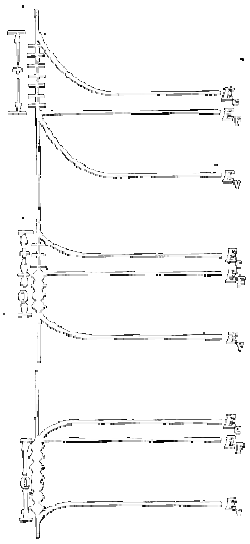
Interface Traps





Traps cause "sloppy" *C-V* and also greatly degrade mobility in channel

$$\Delta V_G = -\frac{Q_{IT}(\varphi_S)}{C_{ox}}$$

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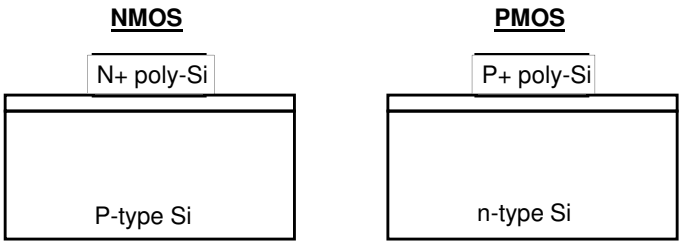
Poly-Si Gate Depletion

A heavily doped film of polycrystalline silicon (poly-Si) is typically employed as the gate-electrode material in modern MOS devices.



- There are practical limits to the electrically active dopant concentration (usually less than $1x10^{20}$ cm^{-3})

$\Rightarrow$ The gate must be considered as a semiconductor, rather than a metal

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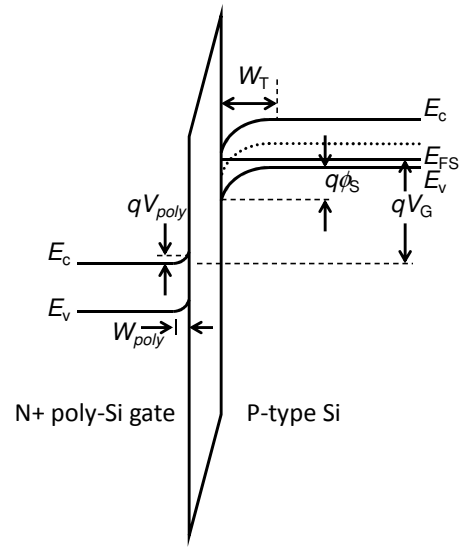
MS Junction (Qualitative)

Si biased to inversion:



V_G is effectively reduced:

$$Q_{inv} = C_{ox}(V_G - V_{poly} - V_T)$$

$$W_{poly} = \sqrt{\frac{2\varepsilon_{Si}V_{poly}}{qN_{poly}}}$$

How can gate depletion be minimized?

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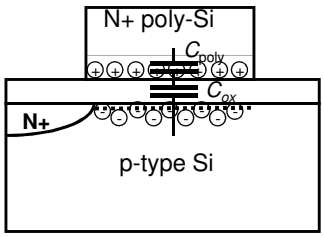
Gate Depletion Effect

Gauss's Law dictates

$$W_{poly} = \varepsilon_{ox}\mathbf{E}_{ox} / qN_{poly}$$



x_o is effectively increased:

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}}\right)^{-1} = \left(\frac{x_o}{\varepsilon_{SiO_2}} + \frac{W_{poly}}{\varepsilon_{Si}}\right)^{-1}$$

$$= \frac{\varepsilon_{SiO_2}}{x_o + (W_{poly}/3)}$$

$$Q_{inv} = (V_G - V_T) \cdot \frac{\varepsilon_{SiO_2}}{x_o + (W_{poly}/3)}$$

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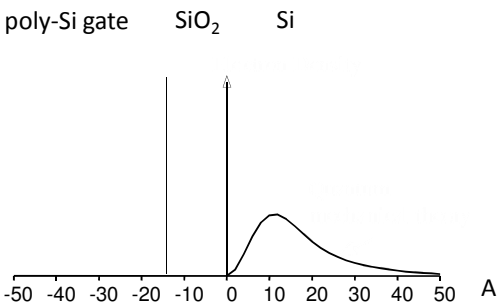
Inversion-Layer Thickness T_{inv}

The average inversion-layer location below the Si/SiO_2 interface is called the ***inversion-layer thickness, T_{inv}***.



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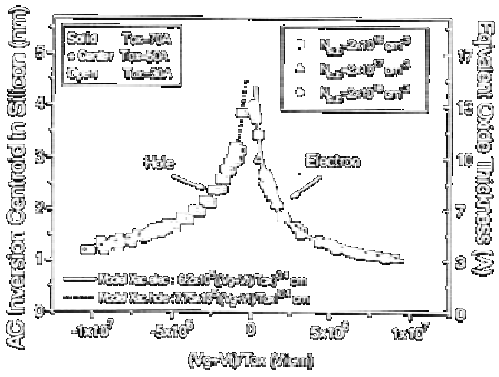
Effective Oxide Thickness, T_{oxe}

$$T_{oxe} = x_o + \frac{W_{poly}}{3} + \frac{T_{inv}}{3}$$ at $V_G = V_{dd}$



$(V_G + V_T)/T_{oxe}$ can be shown to be the average electric field in the inversion layer. T_{inv} of holes is larger than that of electrons because of the difference in effective masses.

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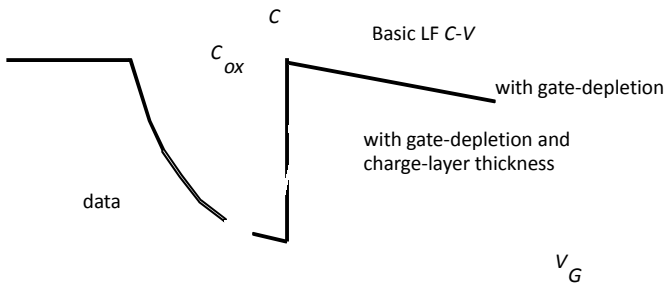
Effective Oxide Capacitance, C_{oxe}

$$T_{ox} = x_o + W_{poly}/3 + T_{inv}/3$$

$$Q_{inv} = \frac{\varepsilon_{ox}}{T_{oxe}}(V_G - V_T) = C_{oxe}(V_G - V_T)$$



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V_T Adjustment by Ion Implantation

- In modern IC fabrication processes, the threshold voltages of MOS transistors are adjusted by ion implantation:
  - A relatively small dose N_I (units: ions/cm^2) of dopant atoms is implanted into the near-surface region of the semiconductor
  - When the MOS device is biased in depletion or inversion, the implanted dopants add to the dopant-ion charge near the oxide-semiconductor interface.

$$\Delta V_T = -\frac{qN_I}{C_{ox}} \qquad N_I > 0 \text{ for donor atoms} \qquad N_I < 0 \text{ for acceptor atoms}$$

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