VLSI Interconnect – HW03 – due 16 Ordibehesht

Consider a transmission line with length x excited with an arbitrary input v_s through a source impedance Z_s and terminated with a load impedance Z_l , as shown in Fig.1. A general transmission line can be considered as a distributed zy (in contrast with distributed rlc) where $z(s)$ is the impedance per unit length and $y(s)$ is the admittance per unit length of the line as shown in Fig. 2.

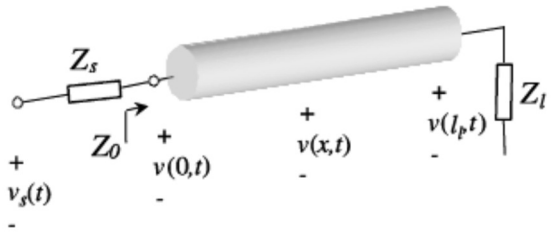

Figure 1

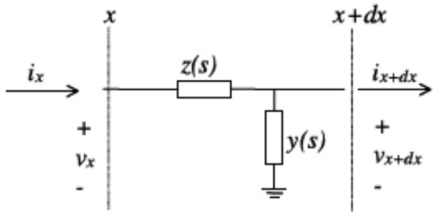

Figure 2

1. Show that the transfer function of a T-line can be written as:

$$H(s) = \frac{v_o(s)}{v_{in}(s)} = k_1(1+k_3)\frac{e^{-\gamma x}}{1-k_2k_3e^{-2\gamma x}}$$

where

$$k_1 = \frac{Z_0}{Z_s+Z_0}\ ;\ k_2 = \frac{Z_s-Z_0}{Z_s+Z_0}\ ;\ k_3 = \frac{Z_l-Z_0}{Z_l+Z_0}\ ;\ \gamma = \sqrt{zy}\ \ ;\ \ Z_0 = \sqrt{z/y}$$

2. As we discussed in the course, normalizing a line ($z(s) = r + sl$, $y(s) = sc$) to a line with unity time-of-flight (T_F) and characteristic impedance makes all equations shorter and comparisons easier. Suppose an rlc line with length x is driven by a source with an impedance of $R_s + sL_s$ and is terminated by a load capacitance C_l. The concepts that are used for the normalization are as follows:

i. An rlc line with length x, can be replaced by $(xr)(xl)(xc)$ line with unity length
ii. Multiplication of all impedances of any linear circuit by a certain value does not change the voltage-voltage transfer function of the system; therefore, all impedances can be multiplied by the reciprocal of characteristic impedance of the line, Z_0,
iii. Finally, time-frequency duality implies that shrinking time by T_F is the same as multiplying all frequencies by the same factor (T_F).

Show that, by using these three concepts, an rlc line with length x can be replaced by and $\tilde{r}11$ line with unity length. The following relations between timing in the original and normalized cases, however, should be considered (all normalized parameters are marked with a tilde sign):

$$\tilde{t} = t/T_F\ \ ;\ \ \tilde{f} = fT_F$$

Other parameters should be also normalized as:

$$\tilde{R}_s = R_s/Z_0\ ;\tilde{L}_s = L_s/T_FZ_0\ ;\tilde{C}_l = C_lZ_0/T_F\ ;\tilde{r} = rx/Z_0\ ;$$

3. Considering skin effect as $z(s) = r + r'\sqrt{s} + sl$, show that normalized $\tilde{r}'$ can be written as

$$\tilde{r}' = r'x/(Z_0\sqrt{T_F})$$

4. For n-tier design, 2 adjacent levels with orthogonal metal levels are called *pair,* and a *tier* is a collection of pairs with the same pitch (p). For an IC designed in 7.5nm Technology based on [1], fill out Table 1. For $\tilde{C}_l$ consider it can be anything from 5 times C_0 up to 20 times C_0 (as given in Table I of [1], $C_0 = 3.45aF$)

Table 1. Results of n-tier design for 7.5 nm node using Copper wires. Lmax is normalized to the gate pitch (1 GP = 0.1178 µm)

	Pitch[nm]	L_max[GP]	$\tilde{r}_{min}$	$\tilde{r}_{max}$	$\tilde{r}'_{min}$	$\tilde{r}'_{max}$	$\tilde{C}_{l\_min}$	$\tilde{C}_{l\_max}$
Pair1	15	42						
Pair2	15	842						
Pair3	24.7	4706						
Pair4	49.1	12202						
Pair5	84.7	25240						
Pair6	191.8	70084						
Pair7	220.7	82863						

5. Consider an rlc line (with no skin effect) is driving with an ideal source ($Z_s = 0$) and is open ended ($Z_l = \infty$). Rewrite the transfer function with the normalized parameters and plot the root locus of the normalized TF for different values of $\tilde{r}$. What is the minimum value for $\tilde{r}$ such that the T-line acts like an rc line (with real roots)? How can this be considered as the minimum length in the original line?

6. (Extra credit) Redo 5, now considering skin effect ($\tilde{r}' \neq 0$). You may plot the toot locus for changes in $\tilde{r}'$ for different values for $\tilde{r}$. Use data in part 4 for choosing reasonable range for $\tilde{r}$ and $\tilde{r}'$.

7. Insert optimal buffer insertion for longest line in [1]:

A. Considering Bakoglu buffer insertion
B. Considering Cascaded buffer insertion

8. (Extra credit) Use SPICE model (taken from PTM website for 7.5nm [2]) compare your delay calculation with HSPICE results for 7.B. Sweep over the optimal distance between buffers and find x_{opt} based on HSPICE results and compare it with 7.B.

[1] Esmat Kishani Farahani, Reza Sarvari, "Design of n-Tier Multilevel Interconnect Architectures by Using Carbon Nanotube Interconnects." IEEE Trans. VLSI Syst. 23(10), 2015.

[2] http://ptm.asu.edu/