VLSI Interconnect – HW04 – due 18 Khordad

1. Consider a multilevel interconnect that exists on both the global and local levels, connecting point A to point B. The schematic of such a configuration is shown in Figure 1. For this HW ignore the parasitic contribution of interconnect vias. Assume the aspect ratio of interconnects in the both levels are equal to one and the wire width in the global level in 4 times of that in the local level.

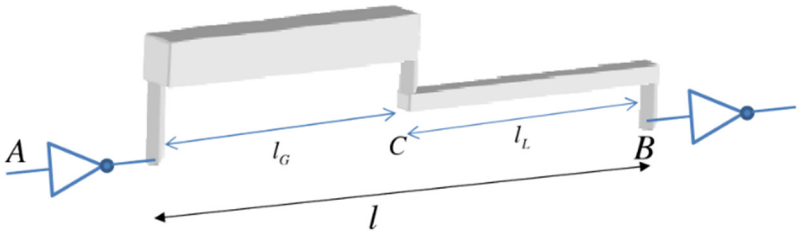


Figure 1

1.1. The parameters r_G, c_G, r_L, and C_L, are the equivalent distributed resistance and capacitance for the global and local levels, respectively. With reasonable assumptions, relate these parameters.
1.2. The parameters R_o, and C_o are the resistance and capacitance of the minimum size driver. Assume the length of the interconnect in the global and local levels are called l_G, and l_L, respectively. Drive an expression for the 50% time delay from point A to B (for the minimum size driver).
1.3. Find point C such that the delay is minimized.
1.4. Assume that a minimum size driver is inserted at point C. Rewrite the delay expression and find point C such that delay is minimized.
1.5 (**Extra Credit**) Assume that the via is passing through Silicon (TSV), the capacitance per unit length of TSV can be written as $C_{tsv} = C_{ox}C_{dep}/\,(C_{ox}+C_{dep})$ where C_{ox} is oxide capacitance and C_{dep} is the depletion capacitance. Assume that for the working voltage $C_{tsv} \approx 0.3C_{ox}$. With reasonable assumptions for r_{tsv}, t_{ox} and l_{tsv} find resistance and capacitance of the TSV. Redo previous parts considering TSV.

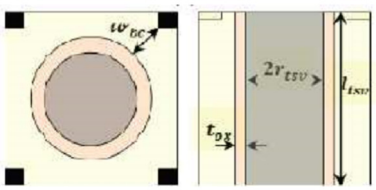


Figure 2

2. Derive a set of coupled differential equations describing the voltage along three neighboring distributed RC lines. Assuming the lines are identical, determine a transformation that decouples these three partial differential equations. Find an input pattern that has a worse case for delay. (**Extra credit** for 4 and 5 coupled lines)

3. Use Sakurai's delay and capacitance formulas to estimate the best-case and worse-case delay for the center conductor in Figure 3. Assume that the minimum size driver output impedance is $R_0 = 4k\Omega$ and the minimum driver input capacitance is $C_0 = 0.7\,fF$. Also assume that the length of the wire is 5mm and is routed on M7. (Use data in Table 1.)

3.1. Without repeaters what is the minimum and maximum delay possible on the center conductor on Fi. 2. Determine the optimal driver size to minimize interconnect delay.
3.2. What is the optimal number of repeaters and optimal driver sizes for this interconnect circuit? What is the new minimum and maximum delay with repeater insertion.

3.3. Is there anything that you could do with repeaters to minimize delay variations? Please explain.

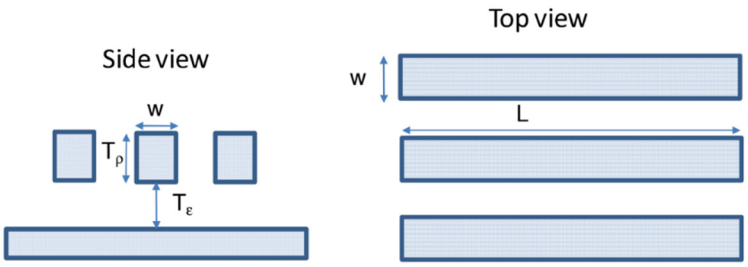


Figure. 3

Table 1. Intel 90nm Multilevel Interconnect Network

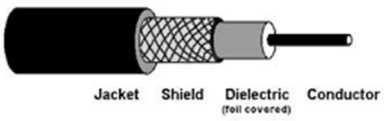
	Pitch(nm) [W+S]	Metal thickness (nm)	Aspect ratio	Lower Dielectric Thickness	Metal width	Metal spacing
Poly	260	140				
Metal 1	220	150	1.4	150	100	120
Metal 2,3	320	256	1.6	256	160	160
Metal 4	400	320	1.6	320	200	200
Metal 5	480	384	1.6	384	240	240
Metal 6	720	576	1.6	576	360	360
Metal 7	1080	972	1.8	972	540	540

Interlevel Dielectric const is k=2.9 and Metal Cu resistivity is $2.2\text{x}10^{-6}$ [Ωcm]

4.

4.1 Prove that signal attenuation along a long is proportional to r/Z_0 .

4.2 Assume that skin-effect loss is dominant for a coaxial cable (as shown in Figure), show that



$$r \propto (\frac{1}{r_1} + \frac{1}{r_2})$$

where r_1 and r_2 are outer and inner radius of conductor and shield.

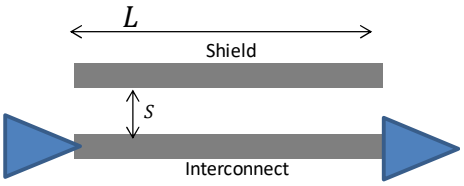
4.3 Find ratio of r_1 / r_2 such that minimizes signal attenuation. Find Z_0 for this condition (assume dielectric constant of 2.23)

4.4 For $Z_0 = 75\Omega$ what dielectric should be used to satisfy minimum signal attenuation condition.

5. (extra credit) Repeat 4 for a PCB line. Pick a high speed board and include board data in your solution. What is optimal Z_0 in your design?

6.1 Consider an interconnect with length L between driver and receiver. This problem is to add shield to the wires. The driver, load, and wire characteristics named as:

$r[\Omega/\mu m]$: resistance per unit length of wire
$R_d[\Omega]$: Driver's output resistance
$C_d[\text{fF}]$: Driver's output capacitance
$C_g[\text{fF}]$: receiver's input capacitance (input resistance is infinite)



The capacitance per unit length of conductor consists of two components:

$C_0 = C_{top} + C_{bot}$ [fF/μm] : capacitance per unit length between top and bottom layers
$C_{lat} = C_{adj}/S$ [fF/μm] : Capacitance per unit length between the conductor and shield (where S is the spacing between the conductor and shielding)

The Fab factory offers only three possible sizes of spacing (S) between the different lines:

$$S_{min} = x \ , \ S_{mid} = 2x \ , \ S_{max} = 3x$$

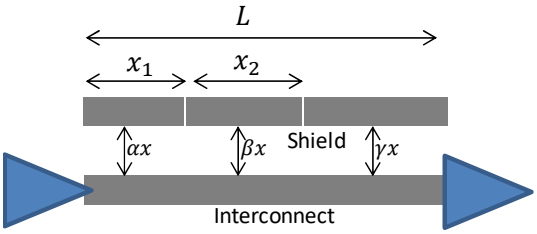
a) Find S, and length which minimizes the delay per unit length of the wire.
b) What spacing minimizes the power dissipation?
c) What spacing maximizes the wiring efficiency?

Repeat a) b) c) neglecting C_d, (justify why we neglect the C_d but not the C_g.)
Express your answers parametrically as a function of C_0 , C_{adj}, x, L, R_d, r .

Given frequency f and supply voltage V_{dd} , what is the difference in power dissipation between these two cases?

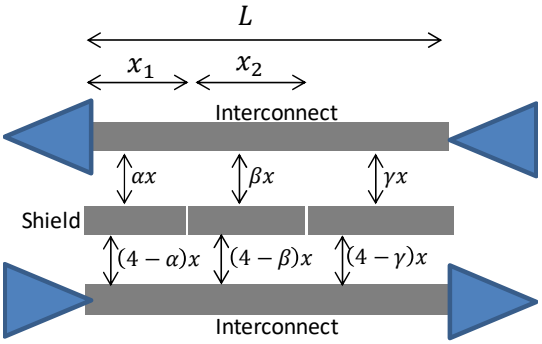
6.2 Now consider $T_{50\%} = const.$ Where that const. is larger than 50% propagation delay of a) and smaller than that of c) . We are interested to minimize the area taking advantage of the possibilities that the plant offers us while keeping the delay constraint.

The following Figure qualitatively describes the realization of the shield in a manner that minimizes the area and will force the Delay. Where $\alpha, \beta, \gamma \in \{1,2,3\}$



Determine the values of α, β, γ which will result in maximal spatial savings while maintaining time constraint. Draw qualitatively and explain your choice. Write down all the required equations to solve the problem of minimization, and explain how to find the refraction points x_1, x_2 (no need to reach the final expression).

6.3 Now, consider a two-way bus with two noisy lines, one line in each direction, separated by a shield line. As shown in the Figure, the distance between the lines is $4x + w_{min}$,(where w_{min} is the shield line's width).



In this part of the question you can ignore the capacitors and resistance of the Buffers, and refer only to the conductors.

Determine the values of α, β, γ which will result in optimal sheilding between the two noisy lines in terms of Delay and power. (qualitatively and explain your choice.) Indicate the Delay equations explicitly, and explain how to find the refraction points x_1, x_2 (no need to reach the final expression).

Is there a difference between a case where the sheild line is connected to V_{dd} and a case in which it is connected to GND?

Do you think there is a possible way to reduce the wasted energy on the parasitic capacitance between the signal line and the shield line?