Short Papers

Crosstalk in VLSI Interconnections

Ashok Vittal, Lauren Hui Chen, Malgorzata Marek-Sadowska, Kai-Ping Wang, and Sherry Yang

***Abstract*— We address the problem of crosstalk computation and reduction using circuit and layout techniques in this paper. We provide easily computable expressions for crosstalk amplitude and pulse width in resistive, capacitively coupled lines. The expressions hold for nets with arbitrary number of pins and of arbitrary topology under any specified input excitation. Experimental results show that the average error is about 10% and the maximum error is less than 20%. The expressions are used to motivate circuit techniques, such as transistor sizing, and layout techniques, such as wire ordering and wire width optimization to reduce crosstalk.**

***Index Terms*—Coupled noise, signal integrity, timing optimization**

I. Introduction

Coupling between signal lines can cause logic failures and timing degradation in digital systems. Such problems become extremely severe in emerging subquarter micron technologies where the neighboring wire capacitance contributions are larger than the contributions due to the effective ground planes (for electric fields) on adjacent metal layers. Besides, high-speed circuits heavily utilize dynamic circuits, which are particularly sensitive to noise at both their input and output lines. The noise coupled onto the input of a dynamic node should be within limits lest an incorrect value be latched leading to repeatable, irrecoverable failures. Further, the outputs of these nodes are not driven and should not be charged or discharged by a leakage path through an adjacent line. With increasing system complexities and the availability of several layers of metal, the number of interactions between signals is large, necessitating automated techniques for constructing layouts without crosstalk problems. Such techniques are the focus of this paper. A preliminary version of this paper was presented at the 1999 International Conference on VLSI Design [17].

There are several tools in existence which extract resistance–capacitance (*RC*) networks from layouts. Simulating the large networks that typically arise is time consuming and it is important to be able to quickly verify that crosstalk on noise sensitive nodes is below the noise margin, or at least identify a much smaller set of nets for detailed crosstalk simulation. The derivation of simple closed form expressions for crosstalk in arbitrary networks has been an open problem for three decades, since [2]. Other relevant research in this area includes the work in [6] and [12] which solves partial differential equations for a pair of lines to arrive at a crosstalk expression. The work in [15] and [16] derives bounds for crosstalk using a lumped model ignoring interconnect resistance, the work in [18] points out that it is important to consider interconnect resistance when computing noise and the research in [3] derives a simple, elegant upper bound for crosstalk under ramp inputs. The peak noise expression in [15] is extended by [13] and [5] to handle resistive interconnects. The essential idea is to introduce equivalent aggressor and victim driver resistances such that the simplicity of the expressions could be maintained. A coupled T network model is used in [13] to extend the expression in [15] to the case of two resistive, capacitively coupled lines. The errors compared to circuit simulation are reported to be less than 20% for the configurations they consider. Similarly motivated work in [5] uses a single pole approximation to derive equivalent resistances for the expression in [15]. Neither [13] nor [5] is guaranteed to yield bounded error. Besides they assume step inputs as in [15]—a clear shortcoming because in the limit of large rise times (compared to circuit time constants), the peak noise is inversely proportional to aggressor input rise time, as shown in [3]. Our results may be viewed as generalizing the result in [15] to handle arbitrary distributed RC networks, under arbitrary input excitation with an arbitrary number of aggressors. Our expressions do not obscure the physical meaning of the various contributions and are simple enough to be used in several formulations, some of which are explored in Section IV. The error of our noise amplitude expression is small even with small rise times, as opposed to the expression in [3] which yields infinite error when rise times are small. Thus, while there have been crosstalk expressions proposed in the past, they have been either for specific configurations or for specific input signals, detracting from their utility in circuit and layout optimization formulations aimed at reducing crosstalk. Our expressions address these shortcomings.

We do not explicitly deal with coupling due to magnetic field interactions in this paper. The magnitude of inductive coupling is small in the presence of good ground return paths close to signal lines. Besides, signals invariably need buffering due to rise time concerns long before line lengths are large enough to warrant coupled transmission line models for crosstalk analysis [9]. Extensions of our expressions for use in underdamped resistance–inductance–capacitance (*RLC*) networks are possible, but are not considered here. We, however, do point out situations where our expressions hold for these cases too.

The paper is organized as follows. Section II derives a measure for noise voltage and an expression for the noise integral for general networks and applies it to several cases. Section III presents results that validate the accuracy and fidelity of these expressions compared to HSPICE simulations on networks obtained from an industrial extraction flow. In Section IV we briefly discuss various circuit and layout optimization problems which can use our new expressions. Section V concludes with a recap of our major contributions.

II. New Crosstalk Expressions

In this section we begin by considering crosstalk in arbitrary extracted networks. Using simple geometric arguments we motivate peak crosstalk noise amplitude and pulse width expressions. We propose their practical approximations to yield simple measures and consider several special cases.

Manuscript received January 1, 1999; revised August 3, 1999. This work was sponsored in part by the National Science Foundation (NFS) under Grant MIP 9811528 and in part by the California MICRO program with contributions from Rockwell Systems and Mentor Graphics Inc. This work was performed when A. Vittal was with Silicon Graphics, Inc. Mountain View, CA, 94043, and L. H. Chen and K.-P. Wang were with Rockwell Semiconductor Systems, Newport Beach, CA, during the summer of 1997. This paper was recommended by Associate Editor C.-K. Cheng.

A. Vittal, K.-P. Wang, and S. Yang are with Synopsys Inc., Mountain View, CA 94043 USA (e-mail: ashok@synopsys.com).

M. Marek-Sadowska and L. H. Chen are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA.

Publisher Item Identifier S 0278-0070(99)09912-1.

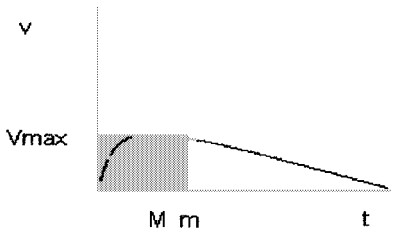


Fig. 1. An arbitrary noise waveform.

Consider a general noise step response s-domain function given by (1). We will generalize to the case of arbitrary input excitation in a later section. There is assumed to be no directly coupled $(s = 0)$ path from input to output, so the zero at $s = 0$ cancels the step input $1/s$. Note that the impulse response is just the expression in (1) multiplied by s

$$V_o(s) = K\,\frac{1 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{1 + b_1 s + b_2 s^2 + \cdots + b_n s^n}. \tag{1}$$

The noise amplitude pulse width product for the frequency domain function in (1) is

$$K = \int_0^\infty v_o\ dt. \tag{2}$$

The effective noise pulse width is

$$b_1 - a_1 = \frac{\displaystyle\int_0^\infty t v_o\ dt}{\displaystyle\int_0^\infty v_o\ dt}. \tag{3}$$

So we propose the "effective" peak noise expression

$$V_p = \frac{K}{b_1 - a_1}. \tag{4}$$

This is equivalent to

$$V_p = \frac{\left(\displaystyle\int_0^\infty v_o\ dt\right)^2}{\displaystyle\int_0^\infty t v_o\ dt}. \tag{5}$$

We motivate the use of V_p with a couple of geometric arguments. A typical noise waveform with median M and mean m is shown in Fig. 1. The mean is

$$m = \frac{\displaystyle\int_0^\infty t v_o\ dt}{\displaystyle\int_0^\infty v_o\ dt}.$$

The median is given by the integral equation

$$\int_0^M v_o\ dt = 0.5\ \int_0^\infty v_o\ dt.$$

Notice that the waveform in Fig. 1 is positively skewed, i.e., the shaded area is larger than the area under the curve until the median. In other words

$$V_{\max} = \frac{\displaystyle\int_0^\infty t v_o\ dt}{\displaystyle\int_0^\infty v_o\ dt} \geq 0.5\ \int_0^\infty v_o\ dt.$$

The expression on the left-hand side is the area under the rectangle (the product of the mean time and the peak voltage) and the right-hand side is the area under the curve from zero until the median (half the total area). This implies

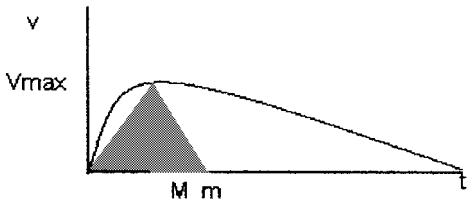


Fig. 2. An expression for $V_{\max}$.

$$V_{\max} \geq \frac{V_p}{2}. \tag{6}$$

Now consider the area of the triangle shown in Fig. 2. The area under the triangle is $V_{\max} * m/2$. Assuming a concave function, the area under the triangle is less than the area under the curve between the origin and the mean m, i.e.,

$$\frac{V_{\max}}{2} m \leq \int_0^m v_o\ dt.$$

As M is the median of the function, the right-hand side of the above inequality can be rewritten as

$$\begin{aligned}\int_0^m v_o\ dt &= \int_0^M v_o\ dt + \int_M^m v_o\ dt \\ &= 0.5\ \int_0^\infty v_o\ dt + \int_M^m v_o\ dt\end{aligned}.$$

Substituting for m and V_p

$$\frac{V_{\max}}{2} \leq \frac{V_p}{2} + \frac{\displaystyle\int_M^m v_o\ dt}{m}.$$

Clearly,

$$\int_M^m v_o\ dt \leq V_{\max}(m - M).$$

Substituting, we get

$$V_{\max} \leq \frac{V_p}{2\,\dfrac{M}{m} - 1}. \tag{7}$$

Thus, $V_{\max}$ lies between $V_p/2$ and $V_p/(2a - 1)$ where a is the ratio of the median to the mean and lies between 0.5 and 1.0 We will see that V_p is a good measure for any optimization formulation which needs a closed form expressions for crosstalk.

In practice, the bounds in (6) and (7) are quite loose. For instance, consider an arbitrary noise response dominated by two poles and normalized such that the area under the curve is unity, i.e.,

$$v(t) = \frac{e^{-t} - e^{-zt}}{1 - \dfrac{1}{z}}.$$

The expression above has to be the form of **any** two-pole response, given that the values at zero and infinite time are zero and the area under the noise curve is unity. It is possible to show that the peak noise for this arbitrary two-pole expression is $z^{1/(1-z)}$ and our peak noise expression is $z/(z+1)$. As z varies from $1+$ to infinity (over the set of all two-pole dominated responses), our expression is actually an upper bound and the ratio of our expression to the true peak noise varies from $e/2$ to 1.0, where e is the base of the natural logarithm. The range of the ratio of our expression to true peak noise is **0.74** to **1.0** for any (not necessarily positively skewed) two-pole dominated noise waveform.

In general, the term b_1 in (4) can be expressed as in [8]

$$b_1 = \sum_{C_i \in C} C_i R_{ii}. \tag{8}$$

C is the set of capacitances, C_i is the ith capacitance, and R_{ii} is the resistance seen across capacitor C_i when all other capacitances are open. In other words, b_1 is the sum of open circuit time constants. The term a_1 in a general network with n nodes takes $O(n^2)$ time to compute. We observed experimentally, on the networks for which we report results in later sections, that a_1 is typically much smaller than b_1. We, therefore, approximate the crosstalk pulse width by b_1 and introduce an approximate peak noise

$$V_p^A = \frac{K}{b_1}. \tag{9}$$

Let us define the Elmore delay [4] of a line, in the presence of coupled parasitics to other lines, to be the first moment of the impulse response, with all other lines to which the network couples to be tied at ground.

We now make a couple of key observations.

Observation 1: The crosstalk pulse width in (9) for a pair of RC lines is the sum of the Elmore delays of the two lines.

Note that b_1 for a pair of coupled RC lines is just the sum of the capacitance-driving point resistance products for all the capacitances in the network. The driving point resistance is defined as the resistance seen across the nodes with all other capacitances open. Consider the sum of the Elmore delays of these two lines, as defined previously. The coupled capacitances appear in the Elmore delay sum expression twice and the corresponding multipliers are the upstream line resistances seen by these capacitances. The sum of the upstream line resistances is precisely the driving point resistance for the coupled capacitance. On the other hand, the capacitances to ground on either line appear only once, with the multiplier being the upstream resistance of the line, which is again the driving point resistance. Thus b1 is precisely the sum of the Elmore delays of the two coupled RC lines.

Equation (9), therefore, relates the peak noise to the delays and will henceforth be referred to as the *noise-delay product expression*.

Observation 2: The noise pulse width for an arbitrary victim net can be computed in linear time.

The sum of ground capacitance-upstream resistance products for a victim can be computed in linear time by a pair of tree traversals [11]. We just need to add the loop resistance-coupling capacitances to get b_1. This is easily achieved by recording the upstream resistances for each victim and aggressor node. From (8), we get the required pulse width.

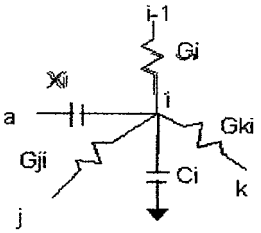
We now state and prove the noise integral theorem.

The Noise Integral Theorem: For a victim tree coupled to n aggressors of arbitrary unit amplitude wave shape, the integral of the noise pulse over time at some node o is

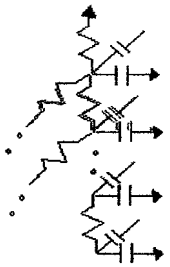
$$K_o = \int_0^\infty v_o \, dt = \sum_{R_i \in P(o)} X_i R_i. \tag{10}$$

The sum is over the set $P(o)$ of resistances in the unique path from the node to the root, X_i is the downstream coupling capacitance at the ith node along the path and R_i is the upstream resistance along this path.

Proof: Fig. 3 shows the elements connected to an arbitrary node in the victim tree and Fig. 3(b) shows the entire network. The victim driver is modeled by its equivalent driver resistance and each node has a coupled capacitance to an arbitrary aggressor node and a capacitance component to ground. The equation characterizing node i in this



(a)



(b)

Fig. 3. An arbitrary node in a victim tree and an arbitrary victim tree.

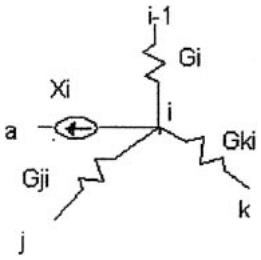


Fig. 4. An analogous network.

network is

$$C_i \frac{dv_i}{dt} + (G_i + G_{ki} + G_{ji})v_i = G_{ji}v_j + G_{ki}v_k + G_i v_{i-1} + X_i \frac{dv_{a,i}}{dt}.$$

Here, C_i, G_i, G_{ji}, G_{ki}, v_i, and X_i are defined in Fig. 3 and $v_{a,i}$ is the voltage across the ith coupling capacitance. Integrating over all time and substituting initial values (all zeros) and final values (one for all aggressor nodes, zero for all victim nodes) for all voltages, we get

$$(G_i + G_{ki} + G_{ji}) \int_0^\infty v_i \, dt = G_{ji} \int_0^\infty v_j \, dt + G_i \int_0^\infty v_{i-1} \, dt + G_{ki} \int_0^\infty v_k \, dt + X_i.$$

The equations characterizing the integral quantities are exactly isomorphic to a resistive network with no capacitors, X_i as the current sources and the same resistors in place, as shown in Fig. 4. The equation characterizing the ith node is

$$(G_i + G_{ki} + G_{ji})v_i = G_{ji}v_j + G_{ki}v_k + G_i v_{i-1} + X_i.$$

The integral quantities in the RC network in Fig. 3 are analogous to the voltages in the resistive network in Fig. 4.

We are interested in the voltage at the output node in the analogous network. Using the principle of superposition, we get the node voltage to be equal to the sum of the current source—driving point resistance products. Hence, the result. □

Notice that the proof depended on the initial and final values of the aggressor lines only and did not make any assumptions about the

wave shape. Thus, the aggressor could have demonstrated overshoot, as in an RLC network, and the result would still hold. Besides, if the logic swing of the aggressor were smaller (as might occur if families with different logic swings are integrated in a system-on-a-chip design), the corresponding term in the noise integral expression would be scaled down appropriately.

We now state and prove the Peak Noise Theorem.

The Peak Noise Theorem: For a victim RC tree coupled to an arbitrary number of aggressors the peak noise measure at any node o is given by

$$V_p^A = \frac{\sum_{R_i \in P(o)} X_i R_i}{\sum_{C_i \in C} C_i R_{ii}}. \tag{11}$$

X_i is the sum of downstream coupling capacitances seen from a node, $P(o)$ is the union of the victim driver resistance and the set of resistances in the unique path from the root to the node o, C is the set of all capacitors, and R_{ii} is the resistance seen across C_i with all capacitors open.

Proof: From the noise integral theorem, we have

$$K = \sum_{R_i \in P(o)} X_i R_i.$$

From (8), we also have

$$b_1 = \sum_{C_i \in C} C_i R_{ii}.$$

The result follows by substituting from the above two expressions into (9). □

The above theorems mean that the product of noise and the delay sum for a pair of RC lines depends only on the victim driver and interconnect resistances and the coupled capacitance. Expression (10) and (11) can be computed in linear time as we noted in Observation 2. Thus our expressions enable optimum time complexity crosstalk verification of layouts as in [15] while considering interconnect resistance and handling arbitrary trees.

A. Handling Arbitrary Input Signals

The expressions in the previous subsection assumed unit step inputs. In this section we remove this assumption and handle the case of arbitrary input excitation. We then show two corollaries for the cases of ramp and saturating exponential inputs.

1) The Nonstep Input Theorem: Consider an arbitrary specified unit amplitude aggressor input function of the form shown in (12). This has to be the form since the initial value is zero and the final value is unity (this follows from the well known initial and final value theorems)

$$V_i(s) = \frac{1}{s} \frac{1 + \alpha_1 s + \alpha_2 s^2 + \cdots + \alpha_m s^m}{1 + \beta_1 s + \beta_2 s^2 + \cdots + \beta_n s^n}. \tag{12}$$

The noise under this input, given a step response represented by (1), is given by

$$V_p = \frac{K}{b_1 - a_1 + \beta_1 - \alpha_1}. \tag{13}$$

Proof: Recall, from Footnote 2, that the noise transfer function has a zero at $s = 0$ and is of the form $sV_o(s)$, where $V_o(s)$ is given in (1). The result (13) follows by multiplying the aggressor input function with the transfer function and making the appropriate identification of the coefficients of s in the numerator and denominator polynomials and substituting into (4). □

The low-frequency zero a_1 may be neglected in (13), as before, if deemed to be expensive to calculate.

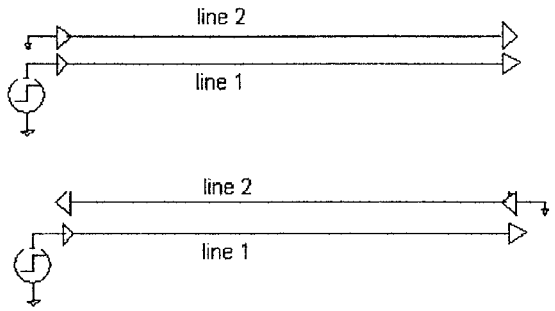


Fig. 5. Noise coupling to far and near-end receivers.

2) The Ramp Input Corollary: Let the input signal be a saturated ramp with rise time T_r, of the form

$$v_i(t) = \frac{t}{T_r}\, u(t) - \frac{t - T_r}{T_r}\, u(t - T_r)$$

where $u(t)$ is the unit step function, so that the noise output function becomes

$$V_n(s) = K\, \frac{1 + \sum_{i=1}^{m} a_i s^i}{1 + \sum_{i=1}^{n} b_i s^i}\, \frac{1 - e^{-sT_r}}{sT_r}.$$

Making a Taylor series expansion for the exponential, so that the noise transfer function reduces to the form in (1) and using our peak noise expression, we get

$$V_p = \frac{K}{b_1 + \frac{T_r}{2} - a_1}. \tag{14}$$

Notice that when the circuit time constants are negligible compared to the input rise time, the peak noise expression reduces to twice Devgan's expression (K/T_r) in [3]. Thus, our expression is a generalization to the case when circuit time constants are not negligible compared to input rise times.

3) The Saturating Exponential Input Corollary: Now consider a saturating exponential input with time constant τ

$$v_i(t) = 1 - e^{-(t/\tau)}.$$

The noise output function becomes

$$V_n(s) = K\, \frac{1 + \sum_{i=1}^{m} a_i s^i}{1 + \sum_{i=1}^{n} b_i s^i} s\left(\frac{1}{s} - \frac{\tau}{1 + s\tau}\right).$$

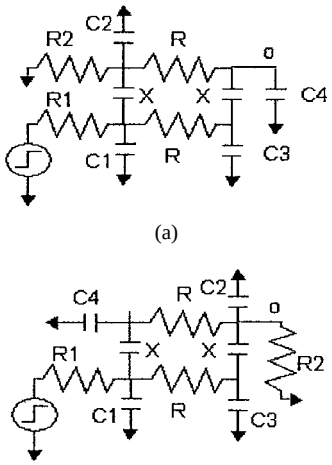
Clearly, our peak noise expression reduces to

$$V_p = \frac{K}{b_1 + \tau - a_1}. \tag{15}$$

B. Special Cases

We will now consider two special cases and show that our expressions reduce to those in [15], when interconnect resistance is negligible. We also show that our expressions for these particular configurations reduce to the expressions of [13] and [5]. Thus, our expression is truly a generalization of these earlier works.

Fig. 5 shows two on-chip lines running parallel on the same metal layer. We wish to compute expressions for the noise voltage on line 2 when line 1 switches. Line 2 is assumed to be quiet (not switching). In particular, we are interested in the peak noise voltage and noise integral at the receiver of line 2.



(a)

(b)

Fig. 6. Equivalent circuits for noise computation.

The equivalent circuits we use are shown in Fig. 6. We have used lumped π models to model the interconnect. However, extensions of the expressions to distributed RC models are straightforward. X denotes half the coupling capacitance and is proportional to the overlap length. C_1 and C_2 are half the line capacitances and C_3 and C_4 are sums of respective half line capacitances and receiver capacitances. R_1 is the aggressor driver resistance, R_2 is the victim output resistance, and R is the line resistance. The victim is in the linear region so a linear model is adequate. The research in [9] shows that a linear model for aggressor driver resistance also models noise surprisingly well, even when transmission line analysis becomes necessary.

Solving the nodal equations for the circuit in Fig. 5(a) to obtain the function V_4 and making the appropriate identification of coefficients, we get

$$b_1 = R_1(C_1 + C_3 + 2X) + R_2(C_2 + C_4 + 2X) + R(C_3 + C_4 + 2X) \quad (16)$$

$$K = (2R_2 + R)X \quad (17)$$

$$a_1 = \left(R_2 \left\| \frac{R}{2}\right.\right)(C_2 + C_3 + 2X). \quad (18)$$

Our peak noise measure becomes the equation shown at the bottom of the page.

When a_1 is neglected in the above expression, it is exactly the expression in [13] and the denominator is identical to that in [5], while the numerator uses an equivalent aggressor driver resistance. We show experimental results in Section III that suggest that even for this special case for which [5] was proposed, our expression yields significantly smaller error. When the interconnect resistance is zero our peak noise measure reduces to

$$V = \frac{2R_2X}{R_1(C_1 + C_3 + 2X) + R_2(C_2 + C_4 + 2X)}. \quad (19)$$

This is exactly the bound in [15]. Thus, the new model shows correct asymptotic behavior when interconnect resistance is small.

For the near-end receiver shown in Fig. 5(b), with the equivalent circuit shown in Fig. 5(b), the expressions for K and b_1 are identical,

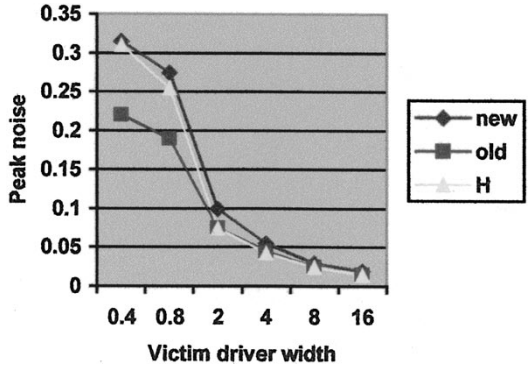


Fig. 7. Model comparisons.

with appropriate correspondences for capacitances, while a_1 is given by

$$a_1 = \left(R_2 \left\| \frac{R}{2}\right.\right)(C_2 + X) + \left(R_2 \left\| \frac{R}{2}\right.\right)\left(1 + \frac{R}{R_2}\right)(C_3 + X). \quad (20)$$

From (18) and (20), we see that a_1 is larger for the near-end configuration, which implies that our noise measure is larger for the near-end configuration. Notice that the circuit equivalent in Fig. 5 corresponds exactly to the type of equivalent circuit obtained for a bus where several lines are routed in parallel for long distances and have no significant noise coupling from the lines running orthogonally on adjacent layers. This suggests that with all else being equal it is best to group all the lines being driven from the left end of a bus together and to clump nets being driven from the right end together. This ensures that nets are subjected to far-end noise, which is smaller. Also notice that neither of the expressions in [5] and [13] have any directionality dependence as they neglect a1. While they do distinguish cases where resistive shielding is important, they fail to capture the directionality dependence.

III. Model Fidelity and Accuracy

In this section we present experimental results which verify the accuracy and fidelity of our expression for peak noise. For a wide range of two-pin and multipin nets, we obtained peak noise using a commercial extraction tool followed by HSPICE simulation using an industrial extraction flow for a 0.35-μm CMOS technology. Notice that all HSPICE simulation results are obtained using the *nonlinear device models* for drivers and receivers and our expressions use the precharacterized linear equivalent resistances. We compare these circuit simulation results to our peak noise expression (9) and the expression in [15], which is essentially (19). Our experiments vary transistor sizes, wire spacing, and the coupling length. About 600 cases have been compared for two-pin nets and about 300 cases for multipin nets.

Fig. 7 shows the variation of peak noise with victim driver transistor width for two-pin nets. The new expression in (9) is always pessimistic, while the expression in [15] can become optimistic because it ignores interconnect resistance. The inter-wire spacing is 0.5μ, the aggressor driver transistor width is 10μ and the coupling length is 100μ. These are fairly typical values within standard-cell blocks.

$$V = \frac{(2R_2 + R)X}{R_1(C_1 + C_3 + 2X) + R_2(C_2 + C_4 + 2X) + R(C_3 + C_4 + 2X) - \left(R_2 \left\| \frac{R}{2}\right.\right)(C_2 + C_3 + 2X)}$$

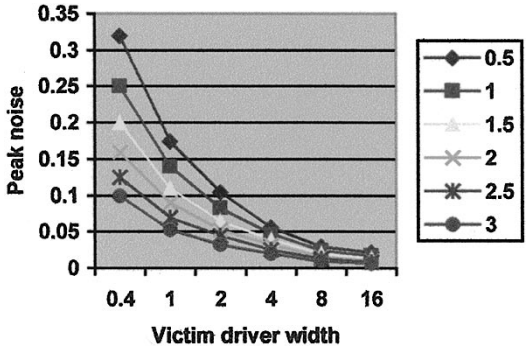


Fig. 8. Wire spacing effects (HSPICE).

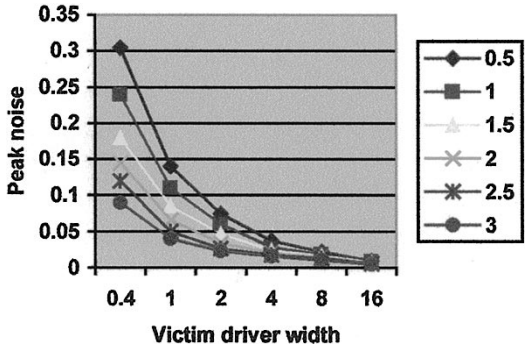


Fig. 9. Wire spacing effects (new model).

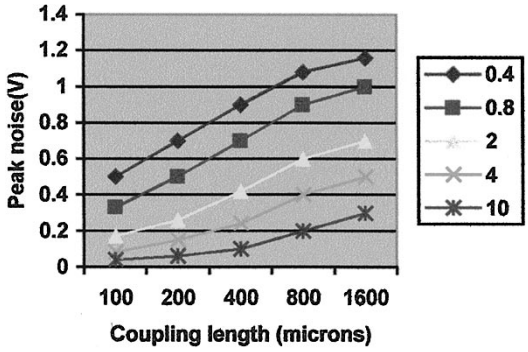


Fig. 10. Noise versus coupling length (HSPICE).

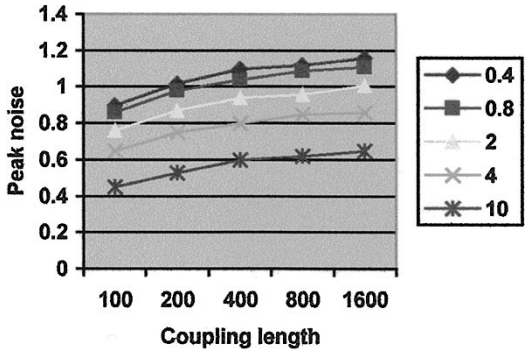


Fig. 11. Noise versus coupling length (new model).

Fig. 8 shows HSPICE results for the variation of peak noise when wire spacing varies from 0.5 μ to 3.0 μ. Fig. 9 shows the same curves using our expression. Notice that our model tracks simulation results.

Figs. 10 and 11 show the variation of crosstalk with coupling length as predicted by HSPICE and our expression, respectively. Both

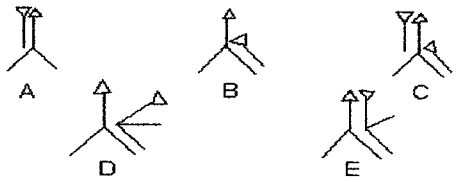


Fig. 12. Multipin topologies.

TABLE I
PEAK NOISE ERRORS FOR MULTIPIN NET TOPOLOGIES

Topology	Average error (%)	Maximum error (%)
A	8.0	15.8
B	8.7	17.5
C	15.6	19.3
D	8.3	13.2
E	8.8	16.1

driver sizing and increased spacing are very effective in reducing crosstalk and our model captures such functional dependence.

We also ran numerous cases of multipin nets of five topologies shown in Fig. 12, with coupling lengths varying from 100 μ to 2000 μ. Table I shows the maximum and average error of the new expression for each topology, compared to HSPICE simulation.

We used our expression and the expression in [3], [5], and [13] to compute the crosstalk for a two-line structure in a 0.35-μm CMOS technology and compared these results with HSPICE. The aggressor and victim driver widths are varied in the range of 0.5μ to 10μ and the coupling length was varied from 100μ to 2 mm. The results are for rise times of 100 ps and 500 ps. In Table II, we show mean and maximum errors of these different expressions.

The results of this section show that our expression tracks HSPICE simulation closely. As our expression is straightforward to compute, it can be used deep within an optimization loop which considers crosstalk. We can also glean important intuition from its simplicity. This is the focus of Section IV.

IV. DESIGN IMPLICATIONS

We use our expressions in formulations aimed at reducing crosstalk in this section. These methods include transistor sizing, wire ordering, wire width optimization and wire spacing.

A. Transistor Sizing

Many performance optimization methods which reduce delay also increase crosstalk an effect which is ignored in classical formulations of timing optimization techniques like transistor sizing [1], [7], interconnect tree topology design and wire width optimization. Our expressions allow these effects to be quantified and included in these formulations. In this section, we generalize transistor sizing to handle crosstalk constraints.

Consider two nets routed in parallel across their entire length as in Fig. 5(a). We pose the problem—what are the optimum driver sizes ($1/R_1$ and $1/R_2$) such that both crosstalk and timing constraints are satisfied? The objective function is the sum of driver transconductances. The zero-noise timing constraints correspond to maximum driver resistances on either line, R_{1m} and R_{2m}. The peak noise constraints are obtained from (9) and correspond to the half-planes

TABLE II
ERROR COMPARISONS OF PEAK NOISE EXPRESSIONS UNDER RAMP AGRESSOR INPUTS

Expression	T_r=100ps		T_r=500ps	
	Average error	Maximum error	Average error	Maximum error
Devgan	12.6	64.4	3.75	19.9
Stohr et al.	0.33	0.63	0.36	0.99
Guardiani et al.	0.07	0.43	0.11	0.67
Ours	0.06	0.33	0.10	0.32

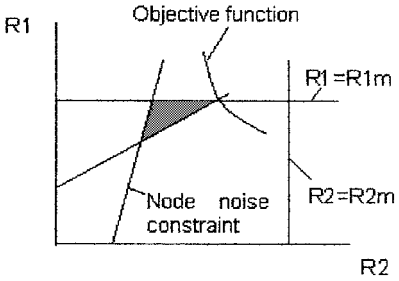


Fig. 13. Transistor sizing with timing and coupling constraints.

TABLE III
WIRE ORDERING AND OPTIMAL SIZING RESULTS

#nets	G_{opt}/G_{min} Random order	G_{opt}/G_{min} New order	Ratio	Run time (s)
10	1.13	1.05	1.11	3.7
50	1.08	1.005	1.08	197

shown. The feasible region is shown in Fig. 13. It is possible to use a sequence of solutions to the linear programming formulation in [1] in order to handle the general problem of n nets with crosstalk constraints. The solution space in the general problem is not bounded by linear polytopes as in the two-net problem. We do not explore the n-net problem here due to space constraints. Details about the use of our expression for transistor sizing appear in [14].

B. Wire Ordering

Consider an on-chip bus. We can reduce the noise by appropriate ordering of the bus bits. This problem was stated in [15] and a heuristic based on a traveling salesperson formulation was proposed, but no results were reported. We propose a new heuristic.

Given any order of bus bits, we can find optimal transistor sizes as indicated in Section IV-A. Our heuristic to find the order begins with the pair of bits which minimizes the sum of transistor sizes. This sequence is then grown by adding a new bit to the existing subsequence, such that the incremental cost (the increase in the sum of transistor sizes) is minimized. Our ordering is compared in Table III to a random ordering followed by transistor sizing using the linear-programming-based method. G_{min} is the sum of transistor sizes without crosstalk constraints. Notice that our bus ordering and sizing enables the handling of crosstalk constraints with less than 5% penalty in the sum of transistor sizes. The wire order for 50 nets essentially achieves crosstalk correctness with virtually no area penalty. The ratio of the sum of transistor sizes when transistors are optimally sized by a random order to the sum when optimally sized following our ordering is around 1.1. Run times for typical bus sizes are reasonable and are for a 200-MHz SGI server running IRIX.

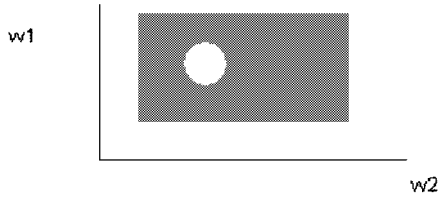


Fig. 14. Wire width optimization with crosstalk and delay constraints.

C. Wire Width Optimization

In this section, we add yet another method to our palette of techniques aimed at crosstalk-correct layout: wire width optimization. Wire width optimization is used for critical signals to increase the line to effective ground plane (on adjacent layers) capacitances such that the coupled noise is smaller. We show that the nonlinear programming problem that arises is nonconvex, so several previous solutions to transistor sizing are rendered inadequate. Note that previous expressions [15] have functional dependence only from the increased line capacitance driven but not the reduced line resistance, so the problem formulation owes its existence to the new expression.

We consider the simple two-wire instance shown in Fig. 5(a) to show that the solution space is nonconvex. We wish to compute wire widths (w_1, w_2) of the two lines such that delay and crosstalk constraints are satisfied. Each of the wires has a minimum technology-specified width and maximum routable width. In classical formulations, we would be interested in finding feasible wire widths such that some cost function is minimized. In the presence of active crosstalk constraints, there exists a closed region within the min-max width rectangle which is infeasible. The feasible region is shown in Fig. 14. The intuitive reason for nonconvex solution space comes from the noise-delay product expression. The crosstalk on a net varies inversely as the sum of the Elmore delays of the two nets. There is an optimum wire width for minimum delay for each net given the load capacitances, driver resistances, and capacitances per unit length. The crosstalk at such a wire width is maximum. Under active crosstalk constraints, a constant delay sum contour in $w_1 - w_2$ space would be a contour of constant crosstalk, thus leading to the nonconvex solution space shown.

D. Wire Spacing Optimization

The formulation in [10] assumes that crosstalk varies as the spacing is changed according to some given linear function of the spacing.

The term in (9) which varies with spacing is the coupling capacitance X. We can use a Taylor series expansion of (9) about the current spacing to obtain the crosstalk as a linear function of spacing. Thus, our expression can be used in the formulation of [10] to space out wires to handle crosstalk constraints.

V. Discussion and Conclusions

In this paper, we have proposed new expressions for peak noise and pulse width in arbitrary topology networks. Our expressions hold for nets with arbitrary number of pins, when driven by any arbitrary specified input excitation. For the special case of victim tree networks, we have shown that our expressions can be easily computed. We showed that our work unifies several of the expressions proposed in past work for crosstalk analysis. Our expressions have been shown to exhibit high accuracy and fidelity compared to HSPICE simulation on several hundreds of networks obtained from an industrial extraction flow. We have also proposed a new formulation for transistor sizing with crosstalk constraints. We have also shown that several other formulations, including wire ordering, wire width and spacing optimization can use our expressions.

References

[1] M. R. C. M. Berkelaar and J. A. G. Jess, "Gate sizing in MOS digital circuits using linear programming," in *Proc. European Design Automation Conf.*, 1990, pp. 217–221.

[2] I. Catt, "Crosstalk (noise) in digital systems," *IEEE Trans. Electron. Comput.*, vol. 16, no. 6, pp. 743–763, 1967.

[3] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects," in *Proc. ICCAD*, 1997, pp. 147–153.

[4] W. C. Elmore, "The transient response of wideband amplifiers," *J. Appl. Phys.*, vol. 19, no. 1, pp. 55–63, 1948.

[5] C. Guardini, C. Forzan, B. Franzini, and D. Pandini, "Modeling the effect of wire resistance in deep submicron coupled interconnects for accurate crosstalk based net sorting," in *Proc. PATMOS*, Oct. 1998, pp. 8.2.1–8.2.10.

[6] H. Kawaguchi and T. Sakurai, "Delay and noise formulas for capacitively coupled distributed RC lines," in *Proc. Asia-Pacific Design Automation Conf.*, 1998, pp. 35–43.

[7] D. Marple, "Optimal selection of transistor sizes in the Tailor system," in *Proc. Design Automation Conf.*, 1989, pp. 43–48.

[8] J. Millman and A. Grabel, *Microelectronics*, 2nd ed. New York: McGraw Hill, 1987, pp. 483–484.

[9] G. Matthaei, J. C.-H. Shu, and S. I. Long, "Simplified calculation of wave coupling in high speed IC's," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 1201–1208, Oct. 1990.

[10] A. Onozawa, K. Chaudhury, and E. S. Kuh, "Performance driven spacing algorithms using attractive and repulsive constraints for sub-micron LSI's," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 707–719, June 1995.

[11] J. Rubinstein, P. Penfield, Jr., and M. A. Horowitz, "Signal delay in RC tree networks," *IEEE Trans. Computed-Aided Design*, vol. CAD-3, pp. 202–211, Feb. 1983.

[12] T. Sakurai, "Closed form expressions for interconnection delay, coupling and crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, pp. 118–124, Jan. 1993.

[13] T. Stohr, H. Alt, A. Hetzel, and J. Koehl, "Analysis, reduction and avoidance of crosstalk on VLSI chips," in *Proc. Int. Symp. Physical Design*, 1998, pp. 211–218.

[14] T. Xiao and M. Marek-Sadowska, "Transistor sizing for crosstalk reduction," in *Proc. ASP-DAC*, 1999, pp. 137–141.

[15] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 290–298, Mar. 1997.

[16] ——, "Reducing crosstalk during routing," in *Proc. Physical Design Workshop*, 1996, pp. 2.2.1–2.2.8.

[17] A. Vittal, L. Hui Chen, M. Marek-Sadowska, K.-P. Wang, and X. Yang, "Modeling crosstalk in resistive VLSI interconnections," in *Proc. Int. Conf. VLSI Design*, Jan. 1999, pp. 470–475.

[18] X. Yang, "Crosstalk-driven layout," masters thesis, Univ. California, Santa Barbara, 1996.